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A Comparative Study of Conventional Multilevel Topologies with a New Single Circuit Topology

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***Abstract*— Multilevel inverter topologies are widely used instead of the two-level H-bridge inverters, especially in high-power medium-voltage applications. But even though they offer reduced harmonic distortion with increase in the number of levels in the output, the major drawback is the increased circuit complexity. So a single circuit with a dc-dc converter and an H-bridge was designed, which can generate various levels in the output with a unique switching technique. This is compared with a cascaded multilevel inverter using MATLAB/Simulink and the results are shown.**

***Index Terms*— Cascaded multilevel inverter, dc-dc converter, H-bridge, Multilevel inverter.**

I. INTRODUCTION

The world today is revived with highly efficient conversion of renewable energy sources with the continued technological advancements in power electronics. It was in 1975 that the concept of Multilevel inverters (MLI) was first proposed, which was a three-level topology. The MLI, as the name suggests, produces an output resembling the shape of a staircase, where each step are different levels of voltage. The major advantage of MLI is that, as the number of steps increases, the output waveform approximates to a sinusoidal shape. The MLI has revolutionized the field of Distributed generation and, the possibility of having an efficient DC-AC conversion at high power range accelerated the researches.

The attractive features of MLIs are as follows:

1. They can generate output voltages with extremely low distortion and lower dv/dt.
2. The input current is less distorted.
3. They generate smaller Common-Mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4. They can operate with a comparatively lower switching frequency.

One drawback with the MLI was the increase in the circuit complexity with the increase in the number of levels. As higher number of levels is necessary, it became practically difficult to handle the large number of power semiconductor switches with associated gate driver circuits. Even though various MLI topologies were developed, each had its own disadvantages and associated problems [1]-[3]. The advantages of having an intermediate DC-DC conversion stage is that only the converter switch operates in the higher frequency and the H-bridge operates in the fundamental frequency so as to generate the AC output [4].

II. CLASSIFICATION OF MLI

The major classifications of MLI are Flying Capacitor (FC) MLI, Neutral Point Clamped (NPC) MLI and Cascaded H-bridge (CHB) MLI. At first, the CHB MLI was defined with a format that connects separately DC-sourced full-bridge cells in series, to synthesize a staircase AC output voltage. CHB MLI was a boon to the medium voltage, high power applications and hence it was used in the industries, especially for Regenerative-type motor drive and utility applications.

A. CHB-MLI

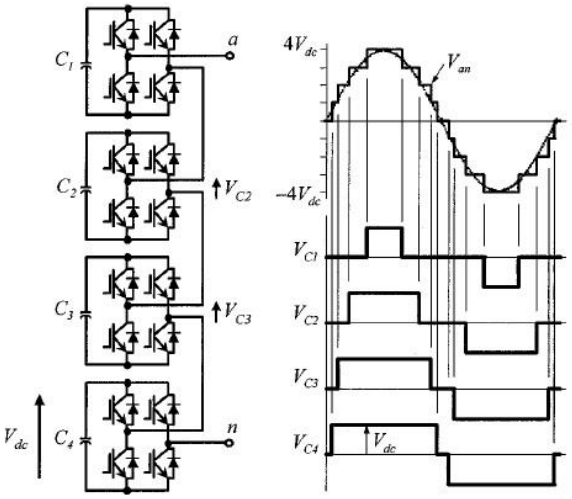

Fig.1. Circuit Diagram of an n-level CHB MLI

Then through the manipulation of the CHB MLI, with the diodes blocking the sources, the diode-clamped MLI was derived [2]. The diode-clamped inverter was also called the NPC-MLI, because when it was first used in a three-level inverter, the mid-voltage level was defined as Neutral point.

B. NPC-MLI

The number of diodes required for each phase will be (n - 1) * (n - 2), (n being the number of levels in output) which makes it impractical to implement for higher number of levels. Also, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications. Since the NPC-MLI was able to double the device voltage level without much voltage matching problem, it was widely accepted and implemented.

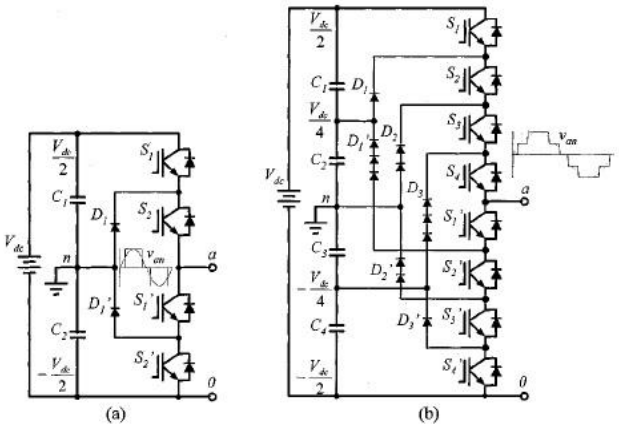

Fig.2. Circuit Diagram of (a) 5-Level and (b) n-Level NPC- MLI

C. FC-MLI

FC was another major MLI, which used independent clamping capacitors for clamping the device voltage to a capacitor voltage. By the proper selection of capacitor combinations, it was possible to balance the capacitor charge.

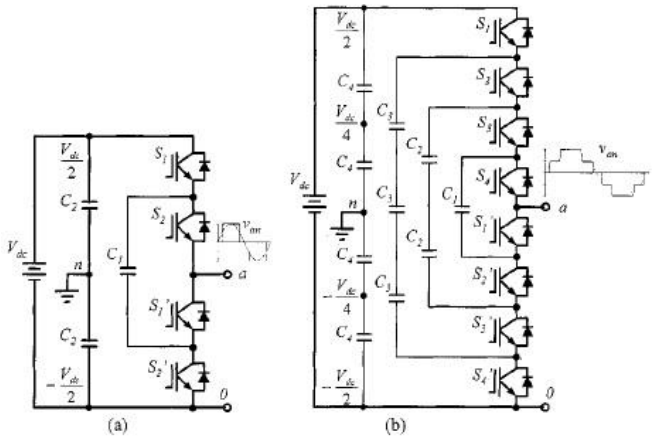

Fig.3. Circuit Diagram of (a) 5-Level and (b) n-Level FC-MLI

But similar to diode clamping, the capacitor clamping requires large number of bulk capacitors to clamp the voltage. It has to be ensured that the voltage rating of each capacitor used is the same as that of the main power switch. An n-level FC-MLI will require a total of $(n-1)(n-2)/2$ clamping capacitors per phase leg in addition to (n - 1) main DC-bus capacitors.

III. PROPOSED TOPOLOGY

A new topology was derived with a two stage conversion, DC-DC-AC where it consists of a Buck converter connected to an H-bridge. This circuit eliminated the problem of increasing circuit complexity with increase in levels, and can easily generate an approximated AC voltage output. The duty cycle of the switch in the Buck converter is varied in the form of m-level Piece Wise Constant (PWC) unidirectional sine wave, to produce a similar output voltage across the output capacitance. The output of the buck converter is an m-level unidirectional sine wave, which is fed to the H-bridge. The switches of the H-bridge operate in the fundamental frequency and hence, generate an n-level AC voltage at its output.

$$n = 2m - 1 \quad (1)$$

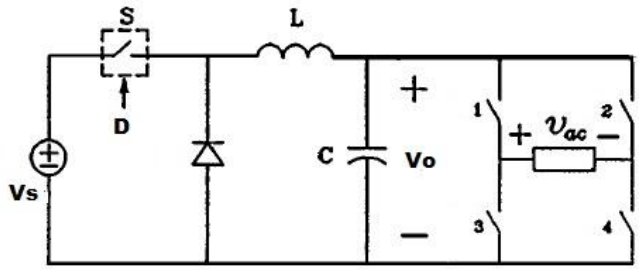

Fig.4. Circuit Diagram of Proposed Topology

The DC-DC converter used is the buck converter and the switch is operated as per the technique which will be discussed next. In this converter, the average output voltage V_o is the product of the duty ratio D and the input voltage V_s, i.e., $V_o = D\,V_s$. As the duty cycle of buck converter is continuously varied, the design is executed in such a way that the output follows this dynamic change. If the input voltage V_s is constant and the duty ratio is varied slowly, relative to the switching frequency in the form of a fully rectified sinusoidal wave, the output V_o will be a fully rectified sine wave. Through a synchronized H-bridge circuit, the output V_o of the converter is unfolded into a sinusoidal waveform V_{ac}. Keeping this in mind, D is derived from a m-level PWC function, such that the Vo will naturally be a unidirectional m-level sine wave. This is made into an n-level AC voltage by the synchronized H-bridge.

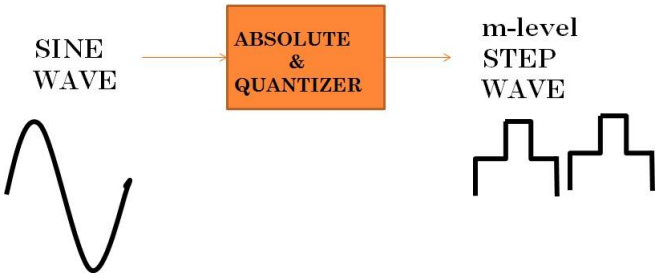

Fig.5. Generation of the m-level step wave

The magnitude and frequency of the output, V_{ac}, are controlled by the duty cycle of dc-dc converter. In order to make the output voltage of buck converter to follow the sinusoidal variation of duty cycle, it is operated in Continuous Conduction Mode (CCM). When the switch is ON, the inductor is getting charged. The step-like variation of duty cycle will ensure a similar step-like output voltage across the output capacitance. When the switch is OFF, the inductance discharges and feeds the load through. This is fed to the H-bridge, and the switching pairs are 1, 2 for the first half and 3, 4 for the next cycle. Because the switches are

operating at the fundamental frequency, it eliminates the possibility of short-circuiting of branches due to commutation failure.

IV. SIMULATION

To show the effectiveness of the proposed topology, a 5-level CHB-MLI is compared with that of the proposed topology. The switching is done using PWM method and a saw tooth waveform is used as carrier. The simulation is done in MATLAB/Simulink and the values are given in the tables below.

Specification	Values
V_{DC}	300V
f_s	35kHz
FF	50Hz
L	1mH
C	10μF
R	5Ω
ΔI_L	0.2A

Table I : Values for the Proposed Topology

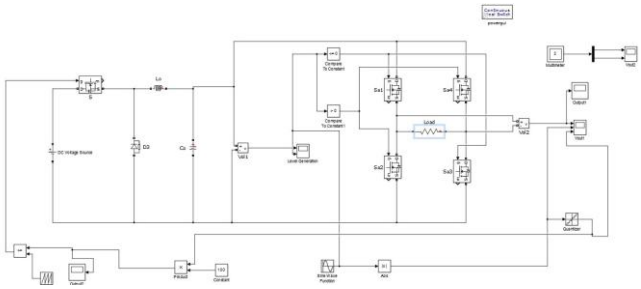

Fig.6. Simulation Diagram for the Proposed Topology

The 5-level output is generated in the proposed topology and the Total Harmonic Distortion (THD) of the output voltage is found out to be 14.37%. The values of the switching frequency and the input DC voltage for the 5-level CHB-MLI are the same. But the THD of the output voltage for the CHB-MLI was found to be 24.14%, which means that the proposed topology is the better option.

The CHB-MLI required cascading of two H-bridges and also two separate DC sources to achieve 5-level, whereas the proposed topology does not require additional circuitry. Also, a 19-level voltage waveform is generated and shown in Fig.10 using the proposed topology.

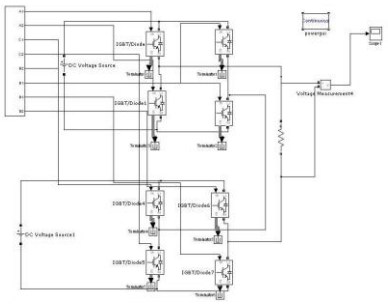

Fig.7. Simulation Diagram for 5-level CHB-MLI

V. WAVEFORMS

The 5-level output voltage and its corresponding m=3 level sine step-wave is shown in the Fig.8.

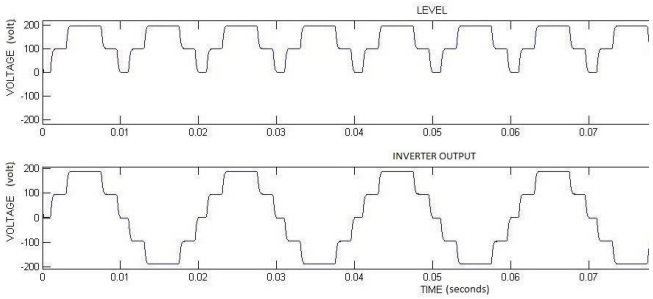

Fig.8. The 5-level Output Voltage and m=3-level Step Waveform of the Proposed Topology

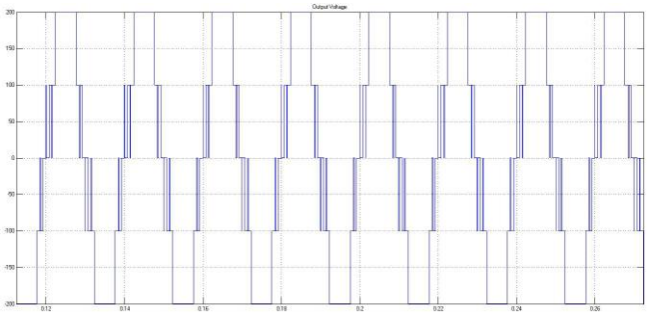

Fig.9. The 5-level Output Voltage of CHB-MLI

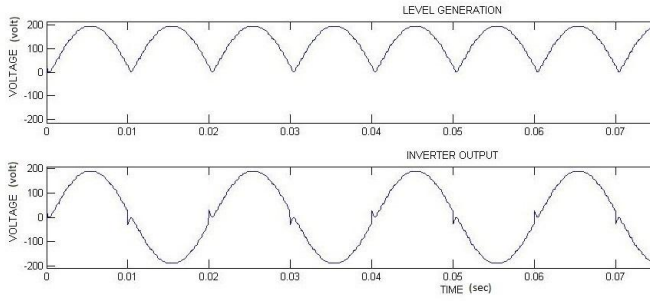

Fig.10. The 19-level Output Voltage and Corresponding m=10 level Step Waveform of Proposed Topology

VI. CONCLUSION

The major classifications of MLI are discussed and the simulation results of one of them were compared with that of proposed topology. By comparing the THD values and the

circuit complexity, the proposed topology looks promising to replace the conventional MLIs.

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