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Post Layout Signal Integrity Test on Verigy Tester Printed Circuit Board

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***Abstract*— The purpose of this manuscript is to do the post layout SI analysis and authentication of loard board that is deliberate for Verigy 93000 tester. The board has been intended to test two DUT's, each has 425 ball pins. The chip has interfaces like PCI, PCIE, GPIO and USB. In this study, single ended signals and PCIe signals have been verified, to observe, if it meets the spec. Post layout SI verification has been carried out to verify the following. Impedance Matching Return & Insertion Loss Analysis Crosstalk Analysis DC/AC Resistance Analysis Propagation Delay Matching (skew) Analysis of Coupled Differential pairs. Interconnect Bandwidth Verification. This analysis can be simulated by Allegro PCB SI.**

***Index Terms*— Signal Integrity Analysis, post Layout Analysis, Verigy tester, Allegro PCB SI**

I. INTRODUCTION

The board has hybrid stackup that uses both Rogers 4350 material and Nelco 4000-13 material. High speed signals like PCIe, USB are constrained to route with the Roger Dielectric. Low speed signals are routed with the elco 4000-13 dielectrics. This kind of hybrid stackup provides advantage of using low dielectric constant, low loss tangent material for high speed signal and also keeping the board cost to minimum by using low cost dielectric for low speed signal.Stackup has been designed for 50 Ohm Single ended impedance. The board thickness is around 160 mils.The layer span is 28 layers with 6 digital layers and 3 analog signal layer. The trace width and the dielectric height to achieve the required impedance are shown below:

II. IMPEDANCE SETUP

Differential signals are designed for 100 ohms differential impedance and trace width and spacing's are controlled as shown below.Requried Impedance will be set before board going to signal integrity analysis. Impedance setup will be shown in below.PCIe signals are routed with 7.5 mils trace width and inter-spacing of 15 mils.Every PCB has a different layer.Our PCB is industry oriented PCB so it has different layers that will be verified first and it will be changed its from original value if its need any modification for proper signal transmission .The Impedance setup eill be shown in below

Subclass Name	Type	Thickness (MIL)	Dielectric Constant	Loss Tangent
	SURFACE			
TOP	CONDUCTOR	1.4	3.800000	0.008
	DIELECTRIC	5	3.800000	0.008
DGND1	PLANE	0.7	3.800000	0.008
	DIELECTRIC	8	3.500000	0.0031
DSIG1	CONDUCTOR	0.7	3.500000	0.0031
	DIELECTRIC	8	3.500000	0.0031
DGND2	PLANE	0.7	3.800000	0.008
	DIELECTRIC	7	3.800000	0.008
DSIG2	CONDUCTOR	0.7	3.800000	0.008
	DIELECTRIC	7	3.800000	0.008
DGND3	PLANE	0.7	3.800000	0.008
	DIELECTRIC	7	3.800000	0.008
DSIG3	CONDUCTOR	0.7	3.800000	0.008
	DIELECTRIC	7	3.800000	0.008
DGND4	PLANE	0.7	3.800000	0.008

Fig.1 Impedance Setup

Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)
	SURFACE	AIR		
TOP	CONDUCTOR	COPPER	1.4	595900
	DIELECTRIC	NELCO_4000_13	5	0
DGND1	PLANE	COPPER	0.7	595900
	DIELECTRIC	ROGERS_4350	8	0
DSIG1	CONDUCTOR	COPPER	0.7	595900
	DIELECTRIC	ROGERS_4350	8	0
DGND2	PLANE	COPPER	0.7	595900
	DIELECTRIC	NELCO_4000_13	7	0
DSIG2	CONDUCTOR	COPPER	0.7	595900
	DIELECTRIC	NELCO_4000_13	7	0
DGND3	PLANE	COPPER	0.7	595900
	DIELECTRIC	NELCO_4000_13	7	0
DSIG3	CONDUCTOR	COPPER	0.7	595900
	DIELECTRIC	NELCO_4000_13	7	0
DGND4	PLANE	COPPER	0.7	595900
	DIELECTRIC	NELCO_4000_13	7	0
DSIG4	CONDUCTOR	COPPER	0.7	595900
	DIELECTRIC	NELCO_4000_13	7	0

Fig.2 Differential signals

From the above figure the different signal that will be presented in vergify tester.

A. Impedance matching

The reflection analysis is carried out to find any potential impedance discontinuity in the design. Stack up has been finalized in the completed design. Reflection analysis is done and the design is verified for positive noise margin, and Ringing. That has been modeled using TDR model and POGO pins are modeled as 50 ohm terminators. Reflection report for the address net taken for DUT 0 is shown below. Positive margins indicate that no significant reflections are present due to impedance mismatch.

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B. *Reflection Report*

Reflection is nothing but when the signal move back to the source when impedance didn't match with input impedance. The below report gives the reflection in the PCB.

Delays (ns), Distortion (mV), (Typ FTSMode)

XNet	NMHigh	NMLow	OShootHigh	OShootLow
1 301928-2218 DUT0_MEM_ADD<12>	382.9	400	982.9	-0.04714
1 301928-2218 DUT0_MEM_ADD<9>	385.7	399.9	985.8	-0.07035
1 301928-2218 DUT0_MEM_ADD<5>	386.9	399.9	987	-0.06648
1 301928-2218 DUT0_MEM_ADD<3>	386.9	399.9	987	-0.05852
1 301928-2218 DUT0_MEM_ADD<4>	388.5	399.9	988.6	-0.03863
1 301928-2218 DUT0_MEM_ADD<6>	388.8	400	988.8	-0.03679
1 301928-2218 DUT0_MEM_ADD<1>	388.8	399.9	988.9	-0.07075
1 301928-2218 DUT0_MEM_ADD<10>	389.3	399.9	989.4	-0.05123
1 301928-2218 DUT0_MEM_ADD<2>	389.6	400	989.6	-0.02783
1 301928-2218 DUT0_MEM_ADD<7>	389.6	400	989.6	-0.04469
1 301928-2218 DUT0_MEM_ADD<0>	391.7	400	991.7	-0.05333
1 301928-2218 DUT0_MEM_ADD<8>	391.8	400	992	-0.03467
1 301928-2218 DUT0_MEM_ADD<11>	391.8	400	991.9	-0.06621

Fig.3 Reflection Report

Pulse analysis also impartant factor in the PCB signal Integrity analysis.The below figure shows the pulse report.

Pulse Data Per Xnet

XNet	PulseFreq	PulseDutyCycle	PulseCycleCount
1 301928-2218 DUT0_MEM_ADD<9>	100MHz	0.5	1
1 301928-2218 DUT0_MEM_ADD<8>	100MHz	0.5	1
1 301928-2218 DUT0_MEM_ADD<7>	100MHz	0.5	1
1 301928-2218 DUT0_MEM_ADD<6>	100MHz	0.5	1
1 301928-2218 DUT0_MEM_ADD<5>	100MHz	0.5	1
1 301928-2218 DUT0_MEM_ADD<4>	100MHz	0.5	1
1 301928-2218 DUT0_MEM_ADD<3>	100MHz	0.5	1
1 301928-2218 DUT0_MEM_ADD<2>	100MHz	0.5	1
1 301928-2218 DUT0_MEM_ADD<1>	100MHz	0.5	1

Fig. 4 Pulse Report

C. *Return and Insertion Loss Analysis*

Dielectric and Skin effect losses dominate in the high speed designs. Return loss and insertion loss analysis are done for high speed PCIe signals, to verify the required eye opening, according to the spec. The following picture shows the eye opening of around 9.5 inch PCIe signal at the receiver, generated with 1000 bits, 10% UI transmitted jitter. The eye opening is around 651 mV which is well above the spec of 175 mV, at the receiver. The maximum length of the PCIe signal has been constrained as 10 inches during Pre layout analysis and the design has been routed with approximately 9.5 inches trace length.

III. EYE DIAGRAM

Mixed mode S parameter was taken for the PCIe differential pairs to determine the performance of the differential pair under the following conditions. Differential signal in-Differential signal out (Insertion loss),Indicates pure differential mode conversion, Differential signal in -Common signal out,Indicates the generation of EMI from the differential pairs,5Common signal in -Common signal out, Indicates the performance of the device under common mode, Common signal in- Differential signal out, Indicates the susceptibility to EMI of the diff pairs, As the following picture shows the differential pair of length 9.5 inches has insertion loss of around -1dB, for common and differential signal inputs.

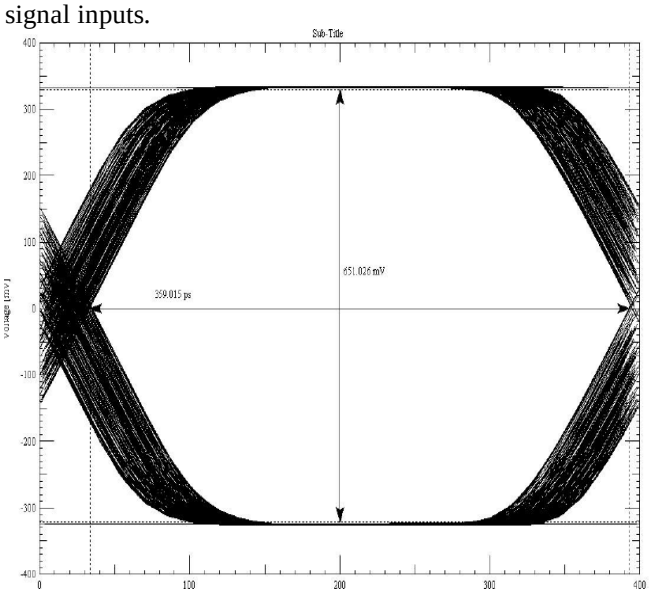

Fig.5 Eye diagram with 1000 bits simulation

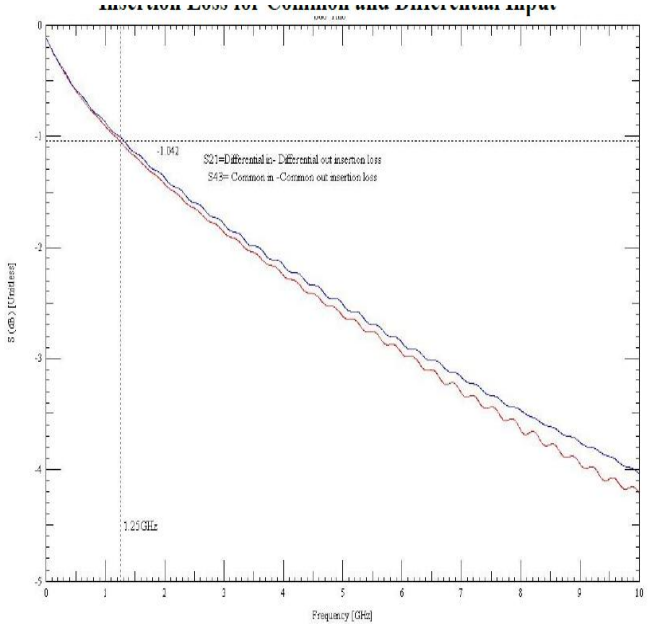

Fig.6 Insertion Loss for Common and Differential Input

Also the above picture shows that, with the value of around -42dB, the PCIe differential pair has well EMI susceptibility and generates less interference

IV. EMI GENERATION AND EMI SUSCEPTIBILITY

The return loss of the 9.5 inch differential pair at 1.25GHz is about -29.9 dB for differential input and -33.495 dB for common mode signal and the picture is shown below.

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A. Differential and Common signal Return Loss

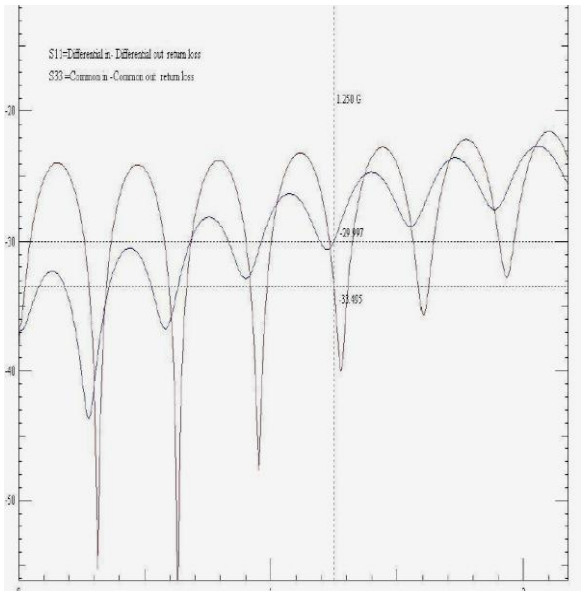

Fig.7 Return Loss

B. Crosstalk Analysis

The single ended traces in the design has been routed with 6.5 mils trace width and minimum spacing of 2x. Following figures shows the NEXT and FEXT of the net DUT0_PCI_AD<0>. Coupled Espice model is extracted from the Layout board to SigXplorer and S parameter has been generated. The NEXT and FEXT value is about -100dB, indicating that the routing for this net is immune to crosstalk. The topology used is shown below.

C. Topology Analysis for Crosstalk Analysis

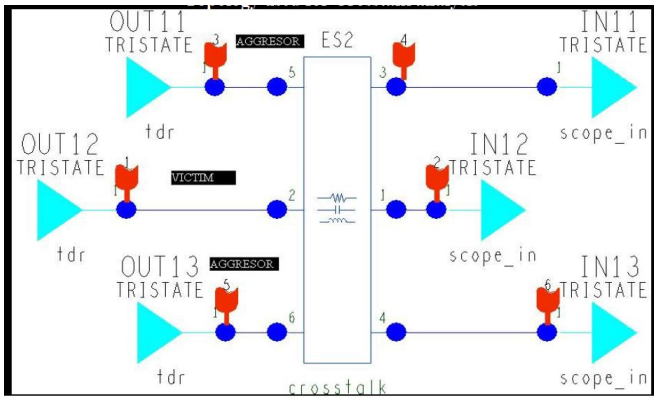

Fig.8 NEXT and FEXT for the net DUT0_PCI_AD<0>

D. DC/AC resistance and Delay Analysis

In order to decrease the losses in the trace, constant impedance and low DC resistance has to be maintained in the routing. The Parasitic report has been taken to verify the AC resistance (Characteristic Impedance) and DC resistance of the nets. Parasitic report and propagation delay of the nets are shown below.

E. Propagation Delay matchuing

Skew between the differential line traces generates common mode current in the return path [3]. In order to control EMI generation, common mode current must be minimized. For PCIe differential signals, skew of less than 30 mils is allowed. The following diagram shows the eye contour of 9.5 inch PCIe signal, routed with skew of around 10 mils. The channel analysis report of PCIe signals simulated with 10E5 bits with 8b10b encoding and 25% UI transmitter jitter is shown below. Eye width of .699 UI and height of 654mV indicates good signal reception at the receiver pins [1].

V. BOARD ANALYSIS

The design has been analysed for three coupled differential pairs, to verify if the spacing between them is sufficient to avoid crosstalk. A snapshot the differential pairs in the layout is shown below

A. Coupled Differential Pairs routed in the Board

Espice model of the three coupled differential pairs are extracted from the board and taken to the SigXplorer, for channel analysis. The differential pairs are routed in the board with 6 mil trace width and 12 mils inter-pair spacing. The minimum intra-pair spacing maintained is 30 mils. The drivers are modeled using Intel 81348 IO processor's PCIe model, so that the results will be comparable to the real world scenario. The Espice topology is shown below.

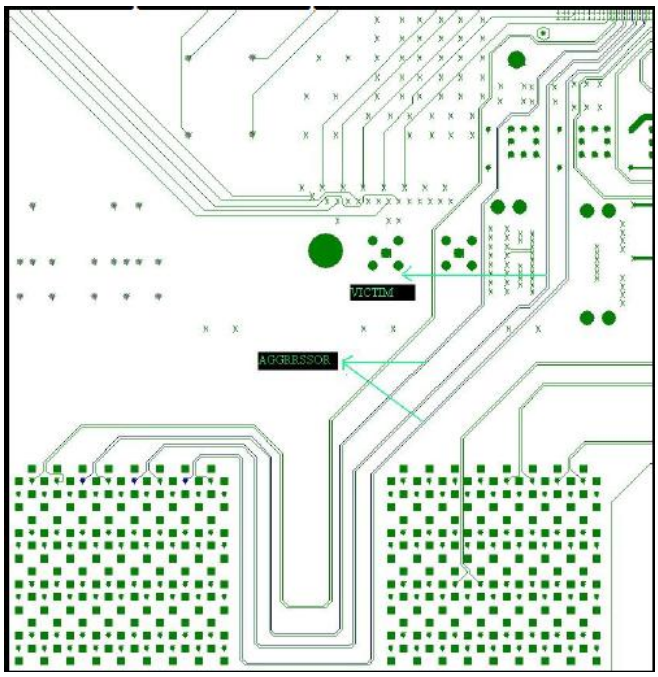

Fig.9 Board Setup

B. Interconnect Bandwidth Verification

Dielectric losses dominate in the Gigabit designs. Bandwidth of the interconnect is increased by Various techniques, such as using equalization technique in case of low cost FR4 material, using low loss tangent materials like Rogers. The -3dB bandwidth of the 9.5 inch PCIe interconnect is about 6 GHz. So this interconnect can transmit the PCIe signals faithfully, from DUT to POGO pins [2].

C. Espice Topology of Coupled Differential pairs

Channel analysis has been done at 2.5Gbps, with 10%UI transmitter jitter and 1E6 bits. The length of the routed interconnect is about 9500 mils. The channel analysis report for odd mode crosstalk is given below.

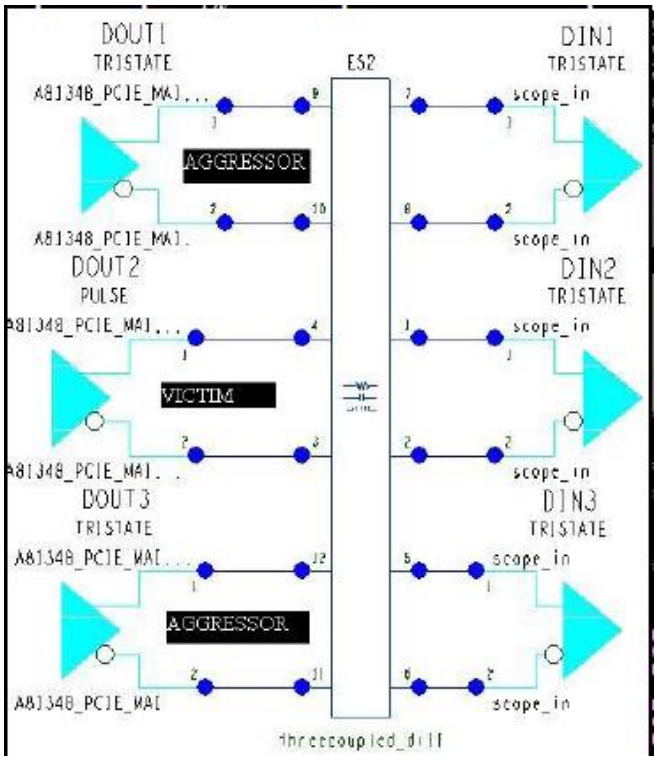

Fig.10 Espice Topology

D. Eye Counter for odd mode crosstalk Channel Analysis

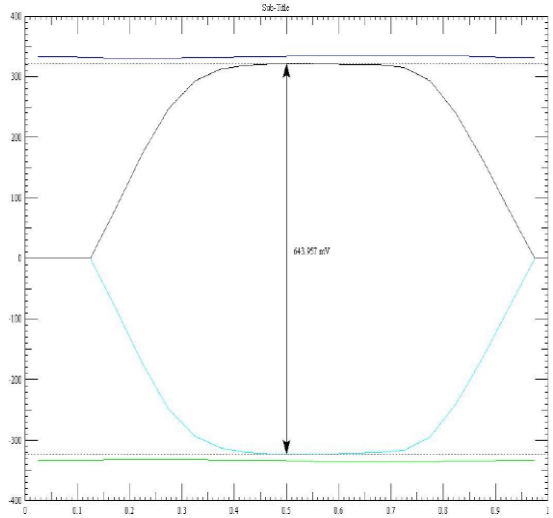

Fig.11 Crosstalk Channel Analysis

VI. CONCLUSION

Detailed analysis has been done for the load board designed for the Verigy 93K tester. Post layout analysis has been done to check if the DUT board performs well, so that the DUT can be characterised accurately in the tester. High speed signal like PCIe, which has got data rate of 2.5Gbps, has been analysed in an elaborate manner with the mixed mode S parameter. Analysis showed that the DUT board will perform well with good Signal integrity for both high speed and low speed signals.

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