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Implementation of Dynamic RAMs with clock gating circuits using Verilog HDL

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***Abstract*--Modern world's major concern is to minimize power consumption by the best way possible. Usage of clock gating technique to minimize dynamic power in sequential circuit is one of the best methods. This paper concentrates on the methods how to restrict the power supply to required sequential circuits rather than supplying to all the components. The design has four RAMs connected to a Demultiplexer along with the clock gating circuit. Their performance on various Xilinx field programmable array platforms has been discussed to emphasis the effect of technique. Total, dynamic and quiescent power of RAM level application of clock gating technique is analyzed. Xilinx ISE design suit 12.2 is used to synthesize, implement and simulate the design.**

***Index terms*--Clock gating, Dynamic power, Power reduction, RAM, DEMUX.**

I. INTRODUCTION

Gadgets became part and parcel of modern man.The effectiveness of electronic devices is maximum if the size, computational complexity and the power consumption are minimum. In past, concentration was on area, cost. But now power consumption is the major concern.

There are five standard techniques to reduce the dynamic power [1].

1. Decrease the average logic-switching frequency.
2. Reduce the propagation of switching activity.
3. Reduce dynamic power by clock gating technique.
4. Lower the capacitance of Routing network, especially for high frequency signals.
5. Use low voltage Input-Output standards.

Almost 30-70% total power dissipation is due to clock signal in synchronous designs [2]. The synchronous design operates at a high frequency that drives a large load because it has to reach many sequential elements. Clock signal do not perform any computation. It is mainly for synchronization. So, it is to be considered the Dynamic power reduction by clock gating technique to eliminate unwanted power loss due to clock signal. Clockgating is a predominant technique to reduce the dynamic power of sequential circuit. Power is saved by clock gating because it adds more logic to prune the clock tree. It can be applied at various levels: system architecture, block design, logic design and gates [3]-[4].

The different techniques to reduce the dynamic power by clock gating technique are [5]:-

1. AND gate based clock gating technique.
2. Latch gate based clock gating technique.
3. Flip flop based clock gating technique.
4. MUX based clock gating technique.

In this paper, Latch free AND gate based clock gating technique is used. This paper presents application of clock gating to four RAM's of various sizes. Different aspects of these modules like simulation, performance results have been shown in this paper. As entire memory is designed to be a positive edge triggered system, It is considered here a Latch free AND gate based clock gating.

In the next section, the proposed methodology is presented followed by results, power comparisons between circuit with clock gating and without clock gating.

II. PROPOSED METHODOLOGY

The block diagram of Latch free AND gate based clock gating circuit which is used as a clock gating circuit is shown in Fig 1.

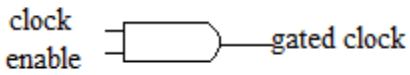

Fig.1.Latch free AND gate based clock gating circuit

As mentioned, two designs one with clock gating and another without clock gating are beenexplained in this section. The traditional power dissipation in sequential logic circuits which does not consist is shown in Fig.2:-

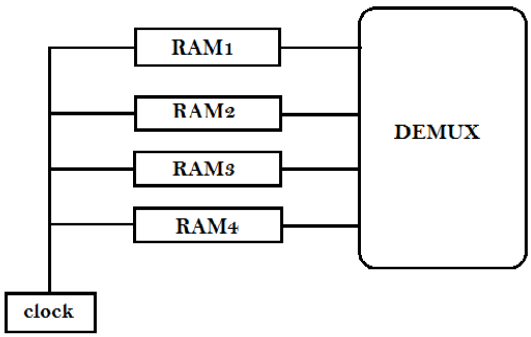

Fig.2.Power dissipation in RAM without CG

In this design, the system clock is directly connected to all Rams. By using the decoder the required RAM can be selected. For instance, if we intend to perform the computations on RAM-2, it is sufficient to send clock signal to RAM-2 only. But here, the clock signal is being sent to all RAMs. In this way power is being unnecessarily dissipated. To avoid this unnecessary power dissipation, clock gating technique is implemented.

The modified design by using clock gating technique is shown in Fig.3:-

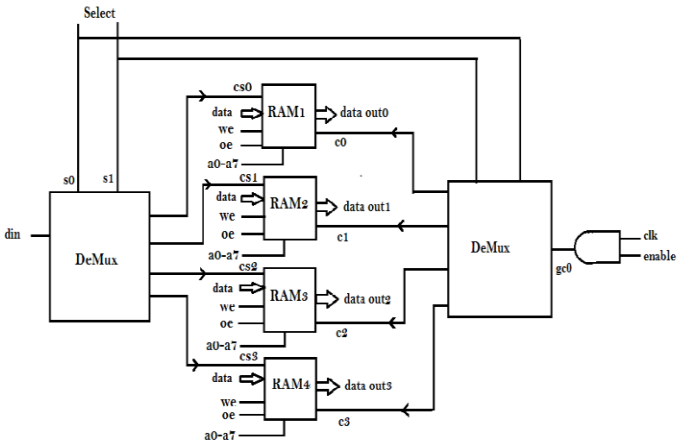

Fig.3.Power dissipation in RAM with CG

In this technique the design is tantamount to the previous one except in the case of clock. Here the clock input is not directly connected.Instead a AND based clock gating circuit which is connected to the circuit using Demultiplexer.For a certain instance of time the clock signal can be supplied to the desired RAM, instead of continuously sending clock signals to all the RAM's.

After simulating the design using the Xilinx ISE design suit 12.2, it is estimated that 97420 kilobytes of memory is used, maximum frequency is 68.138 MHz and Maximum path delay from any node is 3.564ns.

Supply Power Summary(mW):

Total Supply Power	83.04
Dynamic Supply Power	2.03
Quiescent Supply Power	81.01

Design summary:

Logic utilization	**Used**	**Available**	**Utilization**
Total no. of slice registers	388	9312	4%
No. of 4 input LUT's	359	9312	3%
No. of bonded IOB	63	232	27%

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III. RESULTS:-

- Demultiplexer:-

Here the input 'din' willact as enable pin to the demultiplexer.'sel' is selection pin which selects the desired RAM.It is a 2 bit input. Here, 01 is given to 'sel' input to select the RAM-2.

Inputs:-Outputs:-
din=1 cs0=0
sel[1:0]=01 cs1=1
cs2=0
cs3=0

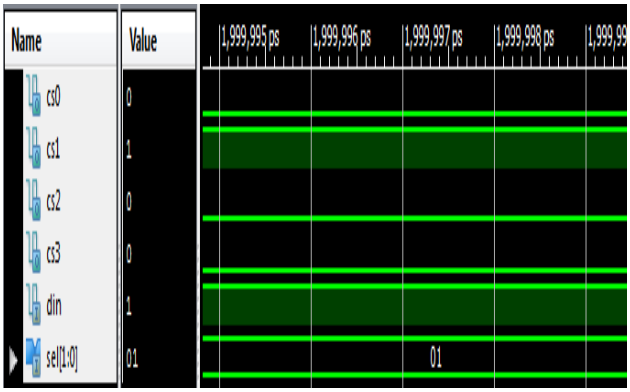

Fig.4.Simulation results of Demultiplexer

- Clock gating circuit:-

Here one of the inputs (clk) is clock signal. The other one is enable signal. These two inputs are given to AND gate.

Inputs:-Outputs:-
clk=1 gc0=1
cs0=1

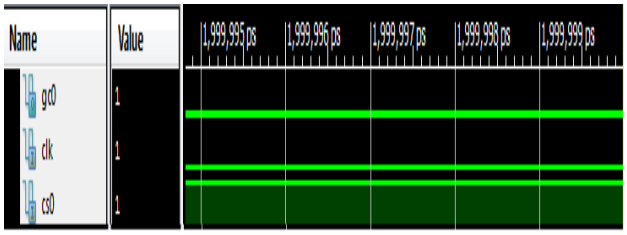

Fig.5.Simulation results of AND based clockgating

- RAM(writing):-

Here we are storing the data 10101010 at the address 00000001 in the RAM-1.

Inputs:- Output:-
cs0=1data_out[7:0]=00000000
we=1
oe=0
gc0=1
address[7:0]=00000001
data[7:0]=10101010

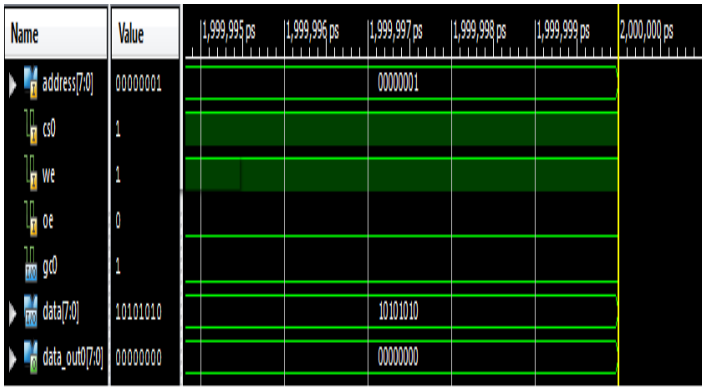

Fig.6.Simulation results of RAM(write operation)

- RAM (reading):-

Here we are reading the data 10101010 from the address 00000001 in the RAM-1.

Inputs:-Output:-
cs0=1 data_out[7:0]=10101010
we=0
oe=1
gc0=1
address[7:0]=00000001
data[7:0]=10101010

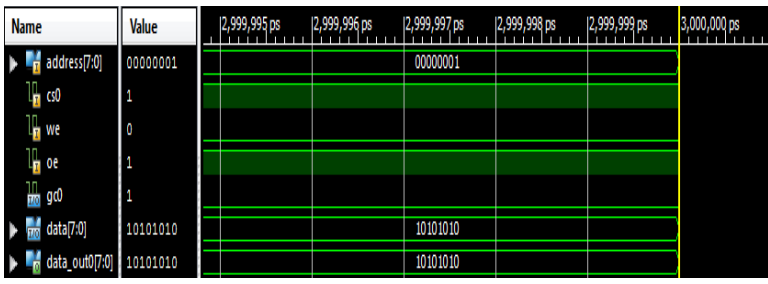

Fig.7.Simulation results of RAM(Read process)

- Main program(writing):-

Out of the four RAM's, we are selecting RAM-1 to store the data 10101010 at the address 00000001.

Inputs:-Output:-
clk=1 data_out[7:0]=00000000
we=1
oe=0
sel[1:0]=01
din=1
address[7:0]=00000001
data[7:0]=10101010

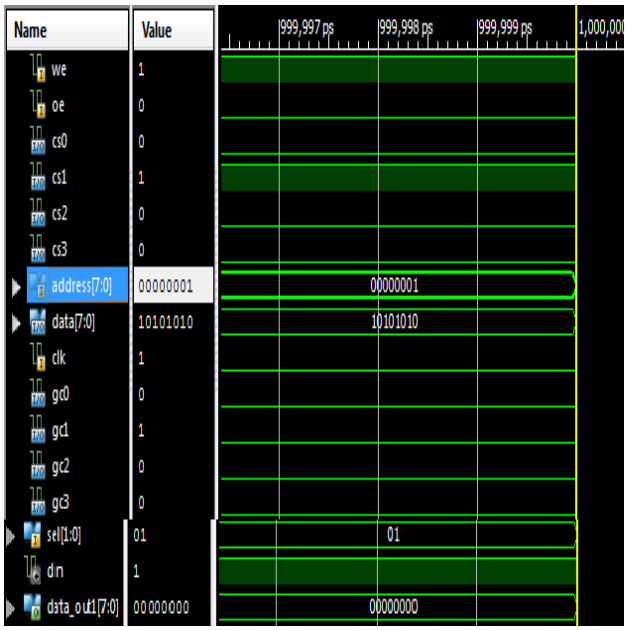

Fig.8.Simulation results of main program (write process)

- Main program(reading):-

Here we are reading the data 10101010 at address 00000001 from RAM-1.

Inputs:- Outputs:-
clk=1 data_out[7:0]=10101010
we=0
oe=1
sel[1:0]=01
din=1
address[7:0]=00000001
data[7:0]=10101010

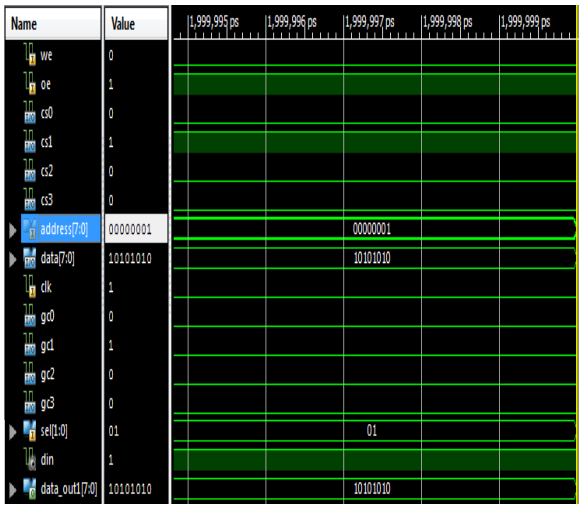

Fig.9.Simulation results of main program (write process)

IV. CONCLUSION

The main aim of this work is to minimize power in synchronous designs by the removal of undesired switching activity using clock gating. This paper has been proposed that clock gating technique has been applied at the RAM level. The selection of one RAM among four RAMs has been done usingdemultiplexer and the clock is given to that RAM using a clock gating circuit and another demultiplexer.
The amout of total, dynamic and queiscent power obtained by the choice of clock gating technique, clock frequency and method of this technique is presented.Clock gating technique can be very handy in designing low power consuming memory by pruning the clock tree. The simulation and synthesis of the design are carried on Xilinx ISE design suit 12.2.

V. REFERENCES

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