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LOW POWER D-FLIPFLOP DESIGN USING 2:1 MULTIPLEXER IN MENTOR GRAPHICS

Suchitra S Jaee, Anuradha S

Abstract— **This enumerates low power, high speed design of D-Flip flop using multiplexer having less number of transistors by 2TG. Multiplexer is a unidirectional device used in any application in which data must be switched from multiple sources to a destination. MTCMOS is one of the most important low power techniques which effectively reduce the leakage power. The MTCMOS operates in two modes – high threshold and low threshold modes. The high threshold mode reduces the leakage power and low threshold mode improves the speed performance. To reduce leakage power in MTCMOS circuits, sleep and sleep bar transistors are operated with high threshold voltages. When sleep input is OFF and sleep bar input is ON, there is no current flow in the low threshold voltage main circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal Mode. This circuit can be designed in Mentor Graphics 130nm technology.**

Index Terms— ***Multiplexer, D-Flipflop, MTCMOS Technique, Low power, Mentor Graphics 130nm Technology.***

I. INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. A 2:1 multiplexer is a basic building block of the "switch logic". The concept of the switch logic is that logic circuits are implemented as combination of switches, rather than logic gate. Multiplexers are used in building digital semiconductors such as CPUs and graphics controller, as programmable logic devices, in telecommunications, in computer networks and digital video. This paper represents the low power dissipation of D-Flipflop based 2:1 multiplexer.

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II. MTCMOS TECHNIQUE

MTCMOS technology provides a solution to the high performance and low power design requirements of modern circuit designs. MTCMOS technology provides the transistors that have low, normal and high threshold voltage. This technology is an effective circuit level technique that provides a high performance and low-power design by utilizing both low and high threshold voltage transistors. Transistor which is connected at the power supply (i.e vdd) increases the performance of the device when it is ON, while transistor connected at the ground side is used to consume less power when transistor is in OFF mode. This project describes a low-power and high speed design for 2:1multiplier circuits with MTCMOS technology. The below diagram shows the circuit of MTCMOS.

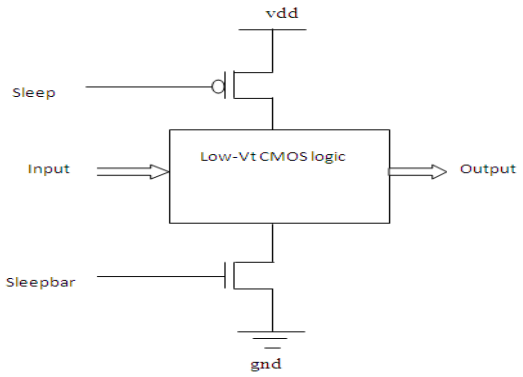

Figure 1: MTCMOS Technique Representation

III. Proposed D-Flipflop based on 2:1 MUX using MTCMOS Technique

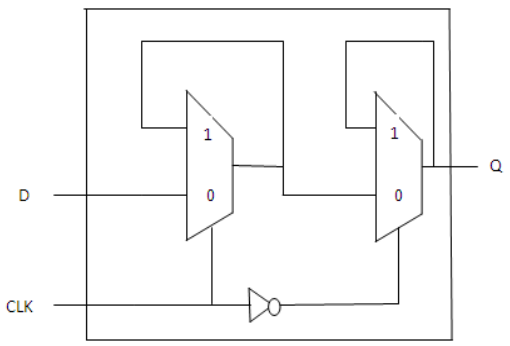

Figure 2: Block diagram of D-Fliflop using 2:1 Mux

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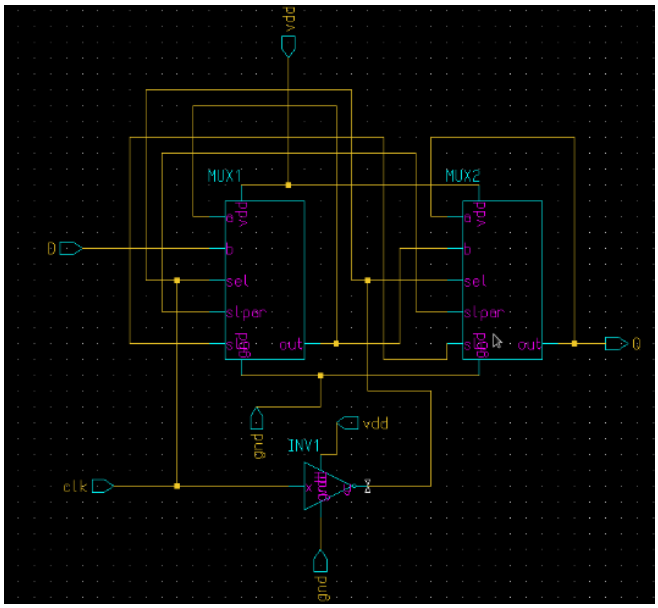

Figure 3: Schematic diagram of D-Fliflop using 2:1 Mux

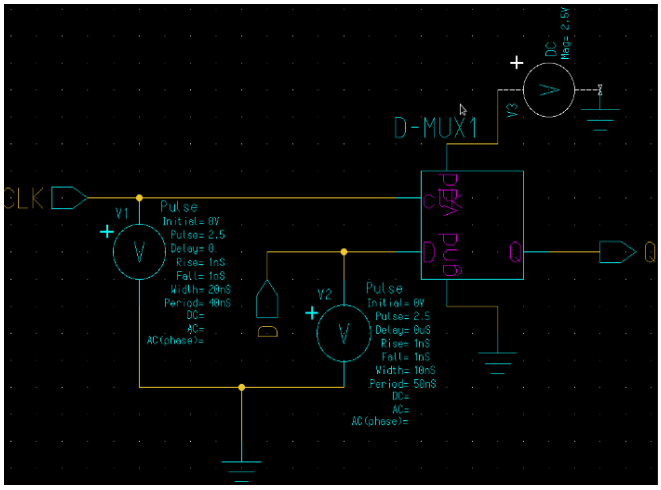

Figure 4: Test circuit of D-Fliflop using 2:1 Mux

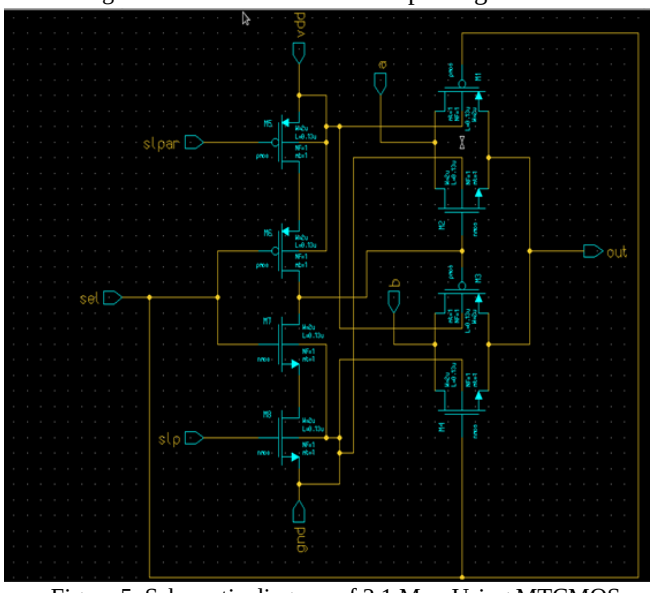

Figure 5: Schematic diagram of 2:1 Mux Using MTCMOS

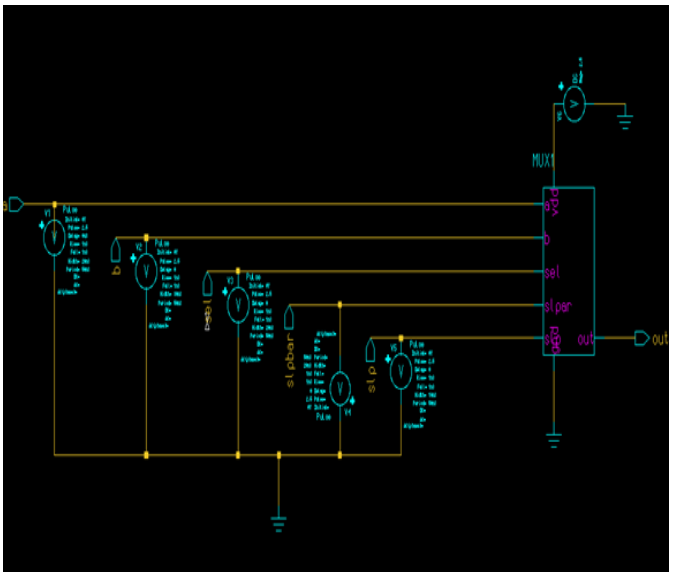

Figure 6: Test circuit of 2:1 Mux Using MTCMOS

The figure 5 shows the schematic of 2:1 multiplexer by using MTCMOS Technique. Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the sub threshold leakage current. A popular low leakage circuit technique is the Multithreshold Voltage CMOS (MTCMOS). The multi threshold CMOS technology has two main features. First, “sleepbar” and “sleep” operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. The transistors having low threshold voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate the low threshold voltage transistors from supply and ground during standby (sleep) mode.

III. SIMULATION RESULTS

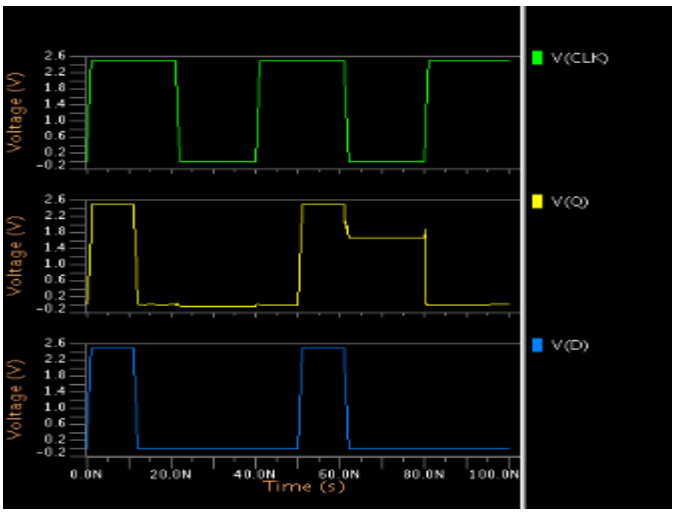

Figure 7: Simulation result of D-Flipflop using MTCMOS

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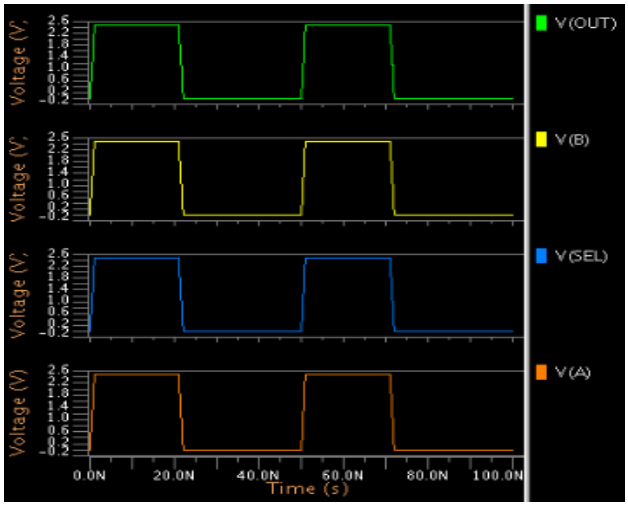

Figure 8: Simulation results of 2:1 Mux

Power Report & System Information of D-Flipflop based on 2:1 Mux using MTCMOS:

```
DC:0 iterations FOR DC analysis
N$17              2.5000
D                 0.0000
CLK               0.0000
Q                 2.1779M
GROUND            0.0000
X_D-MUX1.N$1      1.5249M
X_D-MUX1.N$1    -423.1507N
X_D-MUX1.N$1      5.3325U
X_D-MUX1.X_M     56.9259M
X_D-MUX1.X_M      2.5000
X_D-MUX1.X_M      2.5000
X_D-MUX1.X_M     56.9259M
X_D-MUX1.X_M      2.5000
X_D-MUX1.X_M      2.5000

    TOTAL POWER DISSIPATION:   0.0000       WATTS
***** SYSTEM INFORMATION ...

*** User   : aiet@pc17
*** OS     : Red Hat Enterprise Linux Server release 6.0
*** CPU    :
    Pentium(R) Dual-Core  CPU      E5300  @ 2.60GHz
    Number of physical processors     : 1
    Hyper-Threading Technology        : disabled
    Number of cpu cores               : 2
    Number of logical processors      : 2
*** Freq   : 2600.000MHz
*** Cache  : 2048 KB
*** MEM    : 1020496 kB
*** Date   : Wed Mar 30 11:19:45 2016
```

Power report of 2:1 Mux using MTCMOS:

```
***> DC CPU TIME 0s 000ms <***

DC:1 iterations FOR DC analysis
A   0.0000
B   0.0000
N$22   2.5000
OUT   814.9320P
SB   0.0000
SEL   0.0000
SL   0.0000
X_RULE121.N$12   2.5000
X_RULE121.N$18   56.9890M
X_RULE121.N$20   2.5000

    TOTAL POWER DISSIPATION:   771.4846P    WATTS
```

IV. CONCLUSION

The D-flipflop is designed based on 2:1 Multiplexer in Mentor Graphics 130nm technology. The Simulation results clearly explain the reduction in the power consumption by incorporated with MTCMOS technique. The MTCMOS technique has less power dissipation compared to conventional D-flipflop.

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