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LOW POWER D-FLIP FLOP DESIGN USING AVL TECHNIQUES IN MENTOR GRAPHICS

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Abstract— **Power optimization is a very crucial issue in low voltage applications. This project presents a design of D-Flip flop circuit using AVL techniques for low power operation. It reduces the value of total power dissipation by applying the adaptive voltage level at ground (AVLG) technology in which the ground potential is raised and adaptive voltage level at supply (AVLS) in which supply potential is increased. The main aim of the design is to investigate the power dissipation for D-Flip flop for the proposed design style.**

TSPC based D flipflop has power dissipation of 2.549nwatts. The AVL techniques have less power dissipation. AVLS technique has very less power consumption compared to AVLG (1.3480nwatts) and AVLS technique has very negligible power consumption compared to AVLG. This circuit is designed in Mentor Graphics 130nm technology.

Index Terms— ***Conventional 11T D Flipflop, 5T TSPC D Flipflop. AVL Techniques, Low power, Mentor Graphics 130nm Technology.***

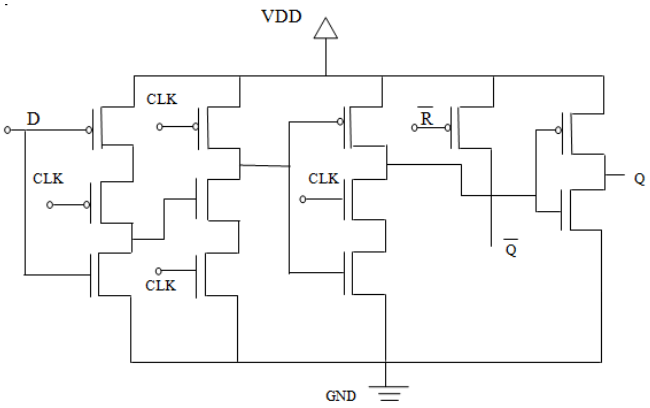
I. INTRODUCTION

Power consumption plays an important role in the present day VLSI technology. Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost. If an IC is consuming more power, then a better cooling mechanism would be required to keep the circuit in normal conditions. Otherwise, its performance is degraded and on continuous use it may be permanently damaged.

II. CONVENTIONAL 11T BASED D-FLIPFLOP

Conventional CMOS D-flip flop circuit consists of alternating stages called n-blocks and p-blocks and each block is being driven by the same clock signal. In this design a single global

clock signal needs to be generated and distributed in order to simplify the design. Figure1 presents positive edge triggered TSPC D-flip-flop. This edge triggered D-flip flop is operated as when the clock signal is LOW, the input is isolated from the output. When clock makes a transition from LOW-to-HIGH the output will latch the complement of the input. During the ON period whatever is the value of input it becomes output. Figure .1 shows the schematic of TSPC D



flip-flop with 11 transistors, this edge triggered flip-flop uses just a single clock signal for synchronization.

Figure 1: 11T Based D-Flip Flop Design

III. 5T TSPC BASED D-FLIPFLOP

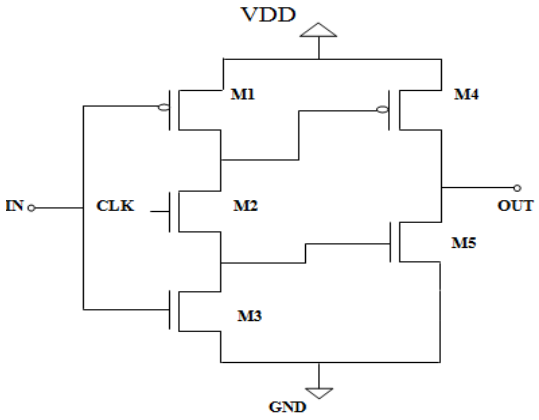


Figure 2: 5T TSPC based D-flip flop.

When CLK and input IN are high then the transistors M1, M5 are OFF and remaining transistors M2, M3, M4 are

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ON. The output becomes high. During ON clock period whatever is the value of input it becomes output.

CLK	IN	M1	M2	M3	M4	M5	OUT
↑	0	ON	ON	OFF	OFF	ON	0
↑	1	OFF	ON	ON	ON	OFF	1
↓	0	ON	OFF	OFF	OFF	OFF	0
↓	1	OFF	OFF	ON	ON	OFF	0

IV. D-FLIPFLOP DESIGN USING AVLG TECHNIQUE

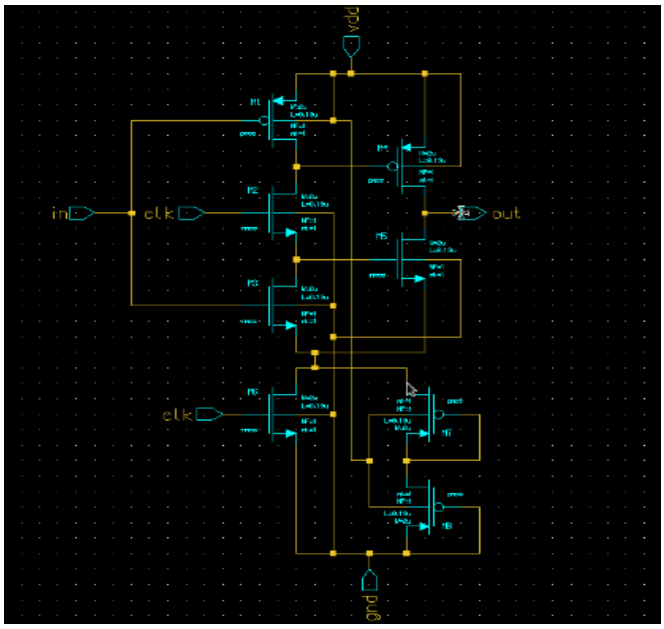


Figure 3: Schematic diagram of D Flipflop using AVLG

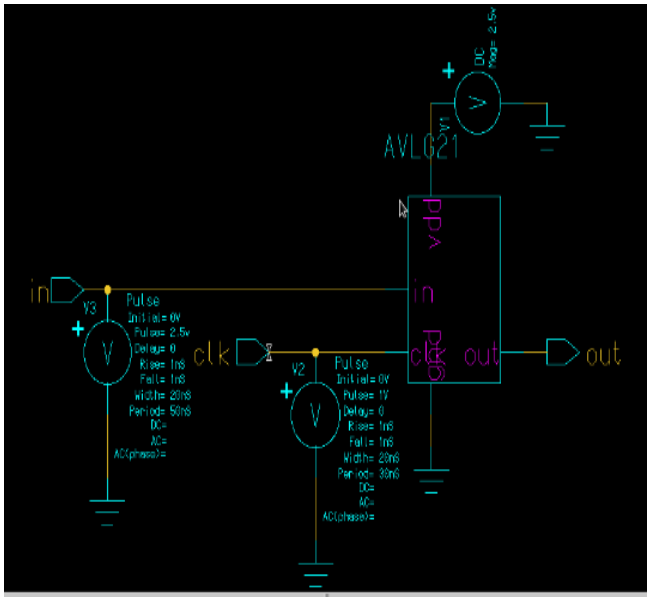


Figure 4: Test circuit of D Flipflop using AVLG

In Adaptive Voltage Level at Supply (AVLS) technique the additional control circuit is made up of combination of 1 PMOS and 2 NMOS transistor connected in parallel. At which an input clock is applied at the input terminal of the PMOS transistor and the rest of the NMOS transistor is connected to the drain terminal. This AVLS control circuit is placed at voltage supply source terminal of the D-flip flop design in which supply is given through this control circuit. This control circuit at the upper end would bring down the supply voltage given to the whole circuit in order to reduce the power consumption of the D-flip flop. When the input is varied corresponding output will be produced. It would reduce the leakage power by reducing the gate to source voltage and gate to drain voltage. This design would be responsible for very low power consumption.

V. D-FLIPFLOP DESIGN USING AVLS TECHNIQUE

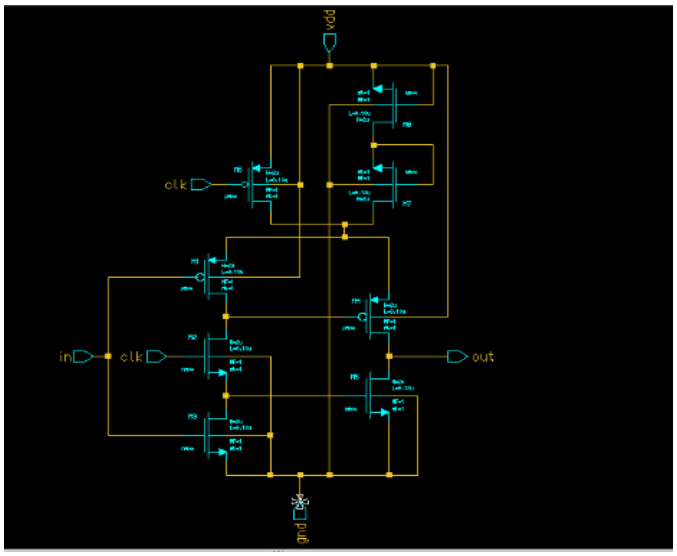


Figure 5: Schematic diagram of D Flipflop using AVLS

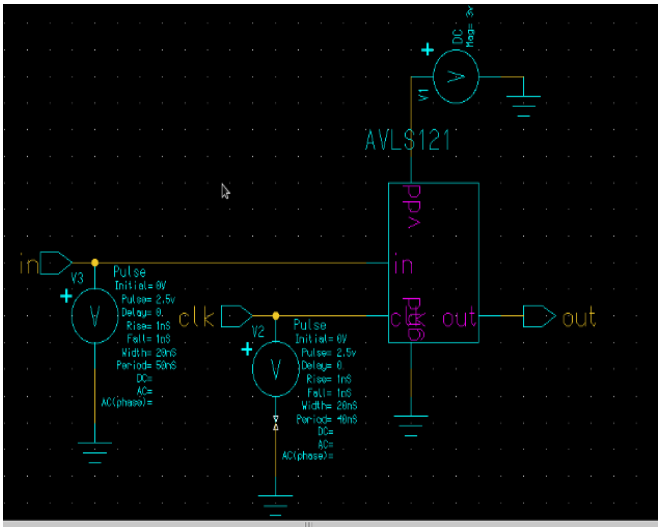


Figure 6: Test circuit of D Flipflop using AVLS

In Adaptive Voltage Level at Supply (AVLS) technique the additional control circuit is made up of combination of 1 PMOS and 2 NMOS transistor connected in parallel. At which an input clock is applied at the input

terminal of the PMOS transistor and the rest of the NMOS transistor is connected to the drain terminal. This AVLS control circuit is placed at voltage supply source terminal of the D-flip flop design in which supply is given through this control circuit. This control circuit at the upper end would bring down the supply voltage given to the whole circuit in order to reduce the power consumption of the D-flip flop. When the input is varied corresponding output will be produced. It would reduce the leakage power by reducing the gate to source voltage and gate to drain voltage. This design would be responsible for very low power consumption.

VI. SIMULATION RESULTS

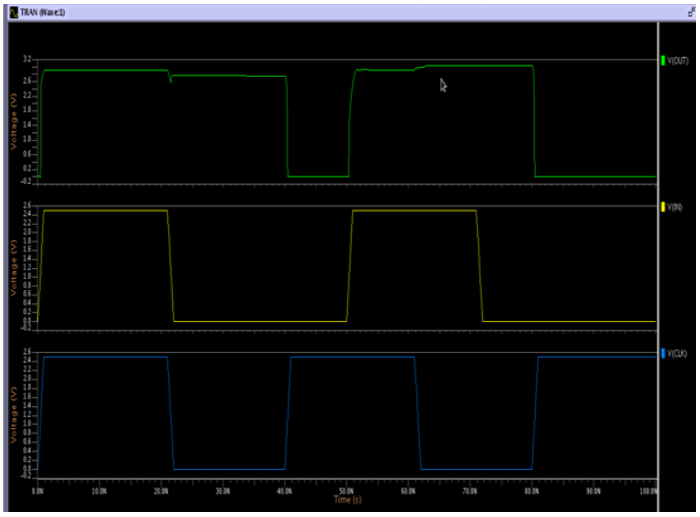


Figure 7: Simulation results of AVLG technique

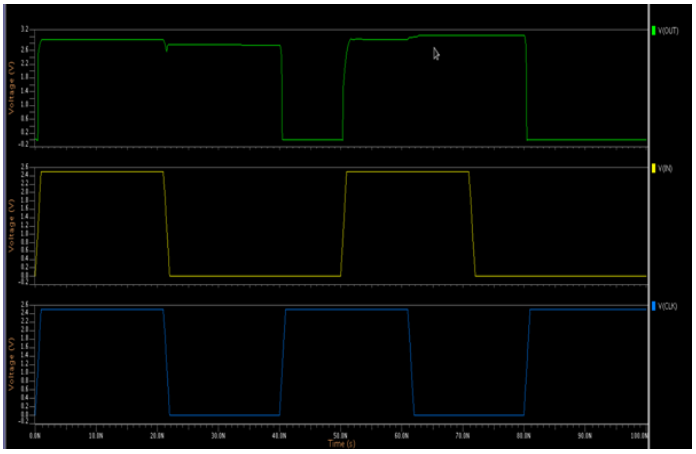
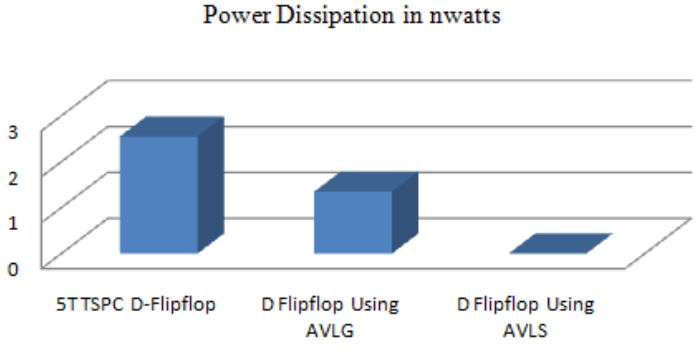


Figure 8: Simulation results of AVLS technique

Power Dissipation in nwatts	5T TSPC D-Flipflop	D Flipflop Using AVLG	D Flipflop Using AVLS
	2.549	1.348	0.000

Table : Power Dissipation




```
DC:6 iterations FOR DC analysis
CLK   0.0000
IN   0.0000
N$6   2.5000
OUT   480.5035M
X_AVLG21.N$12   479.9669M
X_AVLG21.N$2   744.6960M
X_AVLG21.N$27   293.5624M
X_AVLG21.N$4   2.5000

    TOTAL POWER DISSIPATION:   1.3480N      WATTS
```

Figure 9: Power report of AVLG technique

```
DC:0 iterations FOR DC analysis
IN              0.0000
CLK             0.0000
N$9             3.0000
OUT             16.8600M
X_AVLS121.N$    2.6867
X_AVLS121.N$    3.0000
X_AVLS121.N$    66.3346M
X_AVLS121.N$    3.0000
GROUND          0.0000

   TOTAL POWER DISSIPATION:   0.0000      WATTS
```

Figure 10: Power report of AVLS technique

VII. CONCLUSION

The D-Flipflop is designed using AVLG and AVLS low power techniques in Mentor Graphics 130nm technology. TSPC based D flipflop has power dissipation of 2.549nwatts. The AVL techniques have less power dissipation. AVLS technique has very less power consumption compared to AVLG (1.3480nwatts) and AVLS technique has very negligible power consumption compared to AVLG.

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