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A Parallel Architecture Design of Low Power Divide by N using Transmission Gate Logic Circuit

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Abstract: - This paper discusses the low supply voltage area and power optimize counter design using deep sub micron technology. The flip flop circuit design with less number of transistors which uses pass transistor base transmission gate logic. Design using transmission gate reduces the stray capacitances. The design circuit enhances the working frequency due to the reduction of number of transistors, interconnect length, and stray capacitances.In this work the structure of counter compose of three simple CMOS logic modules. An initial module generates predictable counting states for higher significant bit modules through the state look-ahead path. In order to attain high operating frequency a high speed parallel counter is presented.

Index term:-parallel counter, stray capacitance, sub-micron technology, transmission gate

Introduction

The microprocessor, microcontroller and digital signal processor base systems operates on different frequencies. The counter is use as frequency dividers. Counter generate clocks of different frequencies. The n bit cascaded counter counts 2n states and is called as divide by 2n counter. These states are called as modulus of counter. The divide by N counter is the mostly usable module for frequency synthesizers. The circuit propose in this work consist of area and power optimize flip flops with an extra logic which determines the terminal counts and the step size of counting for generation of different frequencies. The circuitry is design is mainly focused on the reduction of complexity of design so that the different frequencies are possible to generate without any design complexity. The transmission gate base Delay flip flop design with 12 transistors as compare to conventional flip flops of 36 transistors. The circuit is design with multiplexer logic structure oftransmission gateinstead of cross connected NAND gate structure.

Literature review

The mostly use frequency dividers are cascaded asynchronous programmable prescaler counters, programmable swallow counters, or programmable divide-by-N counters etc.

In [1] a low voltage and low power divide by N/N+1 counter is design using pass transistor logic technique. A counting and mode selection logic is design with a single transistor in this work with reduced critical path between flip-flops. The divider achieves high-speed operation using a novel parallel counter and a pipelined architecture. The parallel counter is based on a state look-ahead component in conjunction with an internal pipeline structure in order to simultaneously trigger all state value updates without a rippling effect [1].In [2] a digital CMOS high-speed wide-range parallel counter that achieves high operating frequencies through a novel pipeline partitioning methodology is design using state look ahead path logic. It consist of three design modules. An initial module generates anticipated counting states for higher significant bit modules through the state look-ahead path, simple D-type flip-flops, and 2-bit counters. Early design methodologies improved counter operating frequency by partitioning large counters into multiple smaller counting modules, such that modules of higher significance were enabled when allbits in all modules of lower significance saturate. The state look-ahead path is partitioned using the same pipelined alignment paradigm as the counting path and thereby provides the correct anticipated overflow states for all counting stages. Subsequently, all counting states and all

pipelinedDFFs (in both paths) are triggeredconcurrently onthe clock edge, enabling the count state in modules of higher significance to be anticipated by the count state in modules of lower significance [2].The work in [3] introduces the transmission gate logic for leakage and aging optimization. It mitigates the negative bias temperature instability.

Transmission Gates

The CMOS circuit design with transmission gate requires less number of transistors. Transmission Gate has the capability of a high-quality switch with small resistance and capacitance. The structure of transmission gate consists of a source to source and drain to drain connected NMOS and PMOS transistors. The both transistors is turn ON and turn OFF by an enable signal at a time. When the enable signal is at logic '0' then a gate to source potential at NMOS is V and that of PMOS is 5V. This will turn OFF both the transistor. On the other hand for enable signal is at logic level '1' the both transistors are turn ON by this voltage. Thetransmission gate not only reduces the number of transistors but also reduces the number of stray capacitance which in turn reduces power dissipation in the circuit.

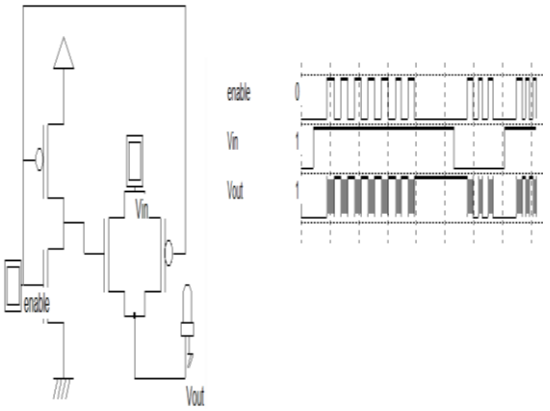

Fig 1 Transmission Gate Logic.

Parallel Counter Architecture

The Parallel counter is design with three basic modules consists of flip-flops and extra logic, which determines the next state of counter. The counterstructureconsistsofthethese trash design modules counts succeeding states through a fixedsetof preassignedcountstates,of which eachsubsequentlycountsterepresents the successive counter value ina chain.

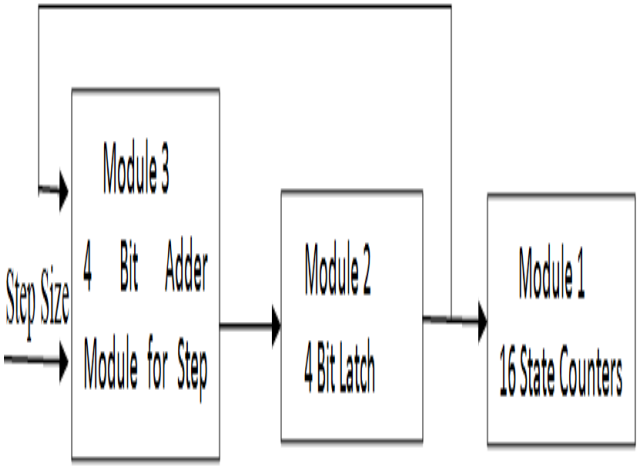

Fig2:Block Diagram ofParallel Counter.

The 16 states counter module is design with a transmission gate base multiplexer logic circuit which work as a 16 states counter logic.Thepurpose of this module isto createall counter in a predefined orderedpositionanditenablefuture statesin successive module-2 'sin conjunction with stimulus from the module3. This counter counts the next state when a stimulusfromthestatemodule 2 four bit latch.The module 1 of 16 states counter design by using transmission gate counts the successive step and the module 2 generates future step size of counting sequence and thus organizes the counting path for these future states. Module 3 is design using 4 bit ripple carry adder in order to decodethe low-order count statesandcarriesthisdecoding over severalclockcyclesinorder totrigger high-ordercountstates.The present state of module 2 is added with the step size input and the next state sequence is generates from module 2.

Timing Simulation, Time-Delay and Power Dissipation and Design Metrics

There are two components that establish the amount of power dissipated in CMOS circuit:

• Static dissipation due to leakage current or other current drawn continuously from the power supply; and

• Dynamic dissipation due to switching of transient current, and charging and discharging of load capacitances.

Dynamic power constitutes the majority of the power dissipated in CMOS VLSI circuits. Thus, for analyzing FA cells only dynamic power is of interest. During a transition from either '0' to '1' or, alternatively, from '1'to '0', both nMOS and pMOS transistors are ON for a short period of time. This results in short current pulse from VDD to GND. Current is also required to charge and discharge the output capacitive load. The current pulse from VDD to GND results in a "short circuit" dissipation that is dependent on the input rise/fall-time, the load capacitance, and the gate design. With no load capacitance, the "short circuit" current is noticeable. As the capacitive load is increased, the discharge or charge current starts to dominate the current drawn from the power supplies. The dynamic dissipation can be modelled by assuming that the rise and fall time of the step input is much less than the repetition period. The average dynamic power (Pd), dissipated during switching for a square-wave input (Vin), having a repetition frequency of fP = 1/tP, is given by

$P_{dynamic} = f\ C\ Vdd^2$

POWER REDUCTION

The power dissipation in MOSFET is

$$P_{avg} = P_d + P_{sc} + P_{leak} + P_{static}$$

Where, P_d is the capacitive switching power dissipation, P_{sc} is the short-circuit power dissipation, P_{leak} is the power dissipation due to leakage currents and P_{static} is the static power dissipation due to non-leakage static currents. Capacitive switching power and short-circuit power are components of dynamic power dissipation. Leakage power is a major component of static power dissipation in CMOS circuits. dynamic power dissipation of a digital CMOS circuit depends on the supply voltage V_{dd}, the clock frequency f_{clk}, the node switching time, the node capacitances, the node short circuit current and the number of nodes. A reduction of each of these parameters results in a reduction of dissipated power. The dynamic power can be reduce byreducing capacitive load which is generated from gate, diffusion and interconnect wiring. This can be done by using pass transistor transmission gate logic which reduces number of transistors and interconnect nodes as possible.

The switching time of CMOS is calculates from its rise and fall time estimation.

The switching speed of CMOS gate is limited by the time taken to charge and discharge the load capacitance CL. An input transition results in an output transition that either charges CL toward VDD or discharges CL toward GND. These are defined as follows:

• Rise-time tr is the time for waveform to rise from 10% to 90% of its steady-state value;

• Fall-time tf is the time for waveform to fall from 90% to 10% of its steady state value; and

• Time-delay td is the time difference between input transitions (50%) and the 50% output level. This is the time taken for a logic transition to pass from input to output.

In order to compare cells in a fair manner, all possible combinations of input patterns and pattern transitions should be applied to a cell. For simulation all eight possible combinations of values of input signals for a FA cell, i.e., 000, 001, 010... 111 are use. An event where one combination of input signals, e.g., 000, to another, e.g., 111, is defined as a transition. Given that our objective is measuring performance of the FA cells with respect to timing behaviour of the cells, we are particularly interested in all possible transitions that can occur. For a FA cell with three inputs (A, B, and Cin) a total of 64 different transitions exist as follows. The combination of input signals 000 has in total eight different transitions as it can go to any of the combinations 000, 001… 111. Similarly, each of the remaining seven combinations of input signals 001, 010… 111 has eight transitions of their own. This makes total of 8x8=64 transitions for all combinations of input signals. In the process of time delay measuring the previous values of the input signals should be considered together with the current signal values. This is due to the fact that there exist cases when the values of input signals remainunchanged implying that the outputsremain

unchanged as well, and, therefore, no time delay should be measured.

For static power dissipation analysis we apply the static input pattern on the circuit and study the leakage power dissipation. The by using variable input pattern the dynamic and average power dissipation is analyze.

Conclusion

Frequency dividers are widely considered as a major limiting factor in frequency synthesizer systems, which require a very fast settling frequency feedback loop and a wide-range of frequency division ratios. Among the most important parameters of high-speed dividers are the operating frequency, operating range, and power consumption. Most modern frequency dividers are typically classified as cascaded asynchronous programmable prescaler counters, programmable swallow counters, or programmable divide-by-N counters. The counter frequency is greatly improved by reducing the gate count on all timing paths to two gates using pass transistor circuit design techniques. In our work the counter operating frequency is varied by using a parallel counter architecture of pass transistor base flip-flops.

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