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Design, Implementation and Analysis Low Power Pulse Decoder for SRAM

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***Abstract*— In SRAM memory, decoder is an important component. To select the particular storage cell and read operation is depend upon the decoder and sense amplifier. In SRAM power dissipation occur in the form of leakage power which is approximately 40% of the total power dissipation. The leakage power of the circuit is increases if we scaling the technology. In this paper design a pulse decoder and simulated the power of the circuit at cadence tool in 45 nm technology. The pulse decoder is designed using two pre-decoder and post decoder with pulsed circuitry. This decoder are design by using AND gate and inverter. Comparison of pulse decoder is done with existing architecture which is design by using three pre-decoders in terms of power dissipation.**

***Index Terms*— Decoder, power, SRAM, Transmission gate.**

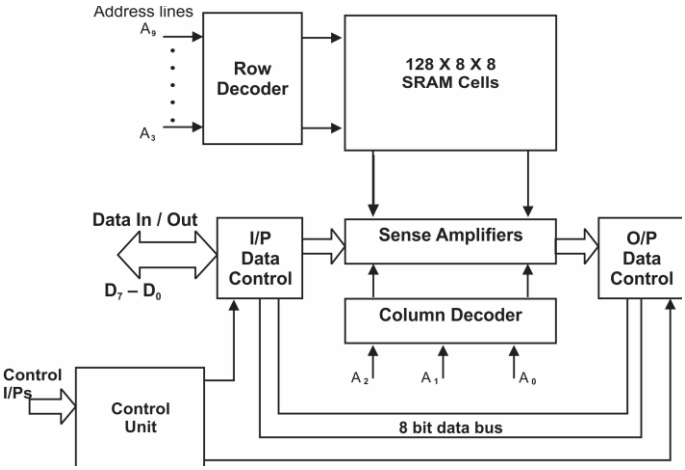

Figure 1: Block Diagram of 128x128 SRAM Cells.

I. INTRODUCTION

In VLSI chips, Fast and low power SRAM is an essential component [1].SRAM is most popularly used as cache memory. As with the improvement in the VLSI technology, if we reduces the length and width of the transistor then supply voltage is reduces and threshold voltage is corresponding reduces. Finally leakage current is increases [2].The main motive is to build out of low power technique for SRAM structure used in processor. Some techniques are used to reduce the power consumption in SRAM like as gated-Vdd, a circuit-level technique to gate the supply voltage and reduce leakage in unused SRAM cells. Their results indicate that gated-Vdd together with a novel resizable cache architecture reduces energy-delay by 62% with minimal impact on performance [3].The dual-threshold technique was used to reduce leakage power by assigning a high-threshold voltage to some transistors in noncritical paths, and using low-threshold transistors in critical path(s)[4]. At architecture state address decoder acts an important role during access time and power consumption is resolve by its design.

The architecture of SRAM is divided into two parts; these are the decoder, the sense and the column circuits. The block diagram of 128 x 128 SRAM cell is shown in Fig 1.It consist of row decoder, a storage array, a column decoder, and a sense amplifier (SA) and write-control unit [5].

A conventional SRAM memory cell made up of pair of inverters these are connected back to back and form a bi-stable element .These inverter are connected to the bit line which are access through pass transistors and they provide the read and write operation. A conventional SRAM memory cell made up of pair of inverters these are connected back to back and form a bi-stable element .these inverter are connected to the bit line which are access through pass transistors and they provide the read and write operation.

An SRAM also contain some row and column circuitry to access these cells. The row decoder and column decoder are used to assert the word line and bit line respectively, correlated address is providing to the input of the circuit. Dynamic decoder having advantages over the static decoder as there speed and power consumption is examining [6]. At Design level some NAND gate design style is used in decoder to reduce the energy consumption and delay [7].

In this paper we design a 5 to 32 word line pulse decoder for a 6T SRAM. The pulse Decoder is designed using two pre-decoder and a post decoder circuitry. The pre-decoder are design using AND gate and NOT gate. The post circuitry consist transmission gate with pulse signal. The design circuit is simulated at 45nm CMOS technology using Cadence Tool. In this paper the proposed pulse decoder is compared with existing architecture using three pre-decoder in terms of power consumption.

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II. CIRCUIT DESIGN OF PULSE DECODER

In SRAM, access path is divided into two parts; they are decoder and the data path. The decoders enclose the circuits from the address input to the word line. The data paths enclose the circuits from the cell to the input/output ports.

In a memory, decoders are used to assert the word lines based on the input addresses. The decoders are designed to drive the capacitance of the word lines. Logically, a decoder is equivalent to n inputs and 2^n output lines. The decoder structure mainly consists of an initial pre-decoder stage, where a group of address inputs are decoded to give the pre-decoder outputs. These are then combined at the next stage to drive the next stage of decoders called post-decoder. In this paper the pulse decoder is design by one 2 to 4 decoder and one 3 to 8 decoder using AND gate and inverter at pre decoder stage. The 2 to 4 decoder and 3 to 8 decoder are shown in Fig 2 and Figure 3 respectively.

In this work AND gate are taken for the decoder design .During the designing of the decoder considered the large inverter for the complete decoder so that it would drive large capacitance of word line. The delay in a circuit is due to the gates follows the critical path. This gate delay of the decoder can be minimized by the pulsed signal is provide to the decoder circuitry.
To access the pulse decoder, some input in the form of signal or binary data are provided. According to the applied input corresponding cell of the memory will be asserted. In decoders based on conventional gates one of the outputs is asserted based on the input address. For next address input the previous output first has to be disable and the new decoder output has to be disable. This operation reduces the speed. This problem can be overcome by using pulsed decoder in which output stays active for a minimum time and then shuts off, a pulse signal shown in figure 4. Here the gates used are conventional but input is given in the form of pulses of short duration So before any access all the word lines are off to be guaranteed and the decoder activates one of the word lines. The critical path of a typical decoder has multiple chains of gates separated by the intermediate interconnect wire. Critical path for a decoder is the longest path from the address input to the output on the local word line. It is important to identify the critical path.

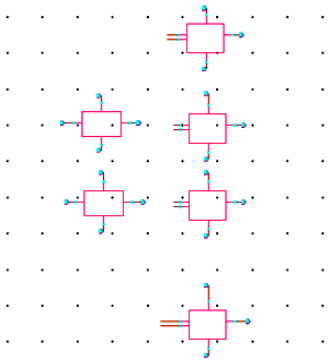

Figure 2: 2 x 4 Decoder.

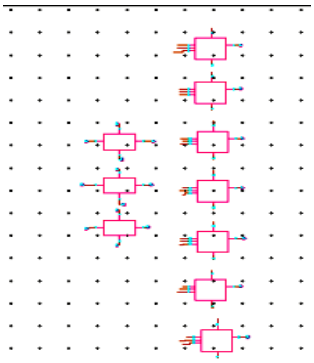

Figure 3: 3 x 8 Decoder.

The pulse decoder is designed using one 2to4 and 3to8 decoder at pre-decoder stage as shown in figure 5. As we increased the numbers of input in the decoder speed of the decoder will be decreases.
Here the decoder design is split into two levels. The first level is the pre-decoder stage which is made up of one 2 to 4 decoder and one 3 to 8 decoder. A Pre-decoder is used in the circuit design to reduce the fan in.
The next level is post-decoder in which all the outputs from pre-decoder are collect to form a total of 32 word lines. Reduce the logical effort of the complete path by splitting the decoder into two stages as shown in figure 5. Using 2 to 4 decoder and 3 to 8 decoder forms the 8 inputs for the pulse decoder.

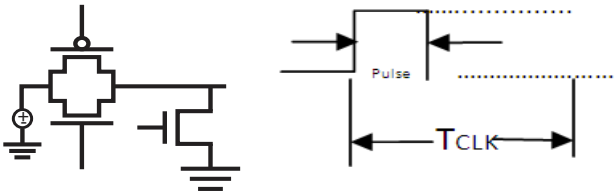

Figure 4: Pulse Circuit with pulse output.

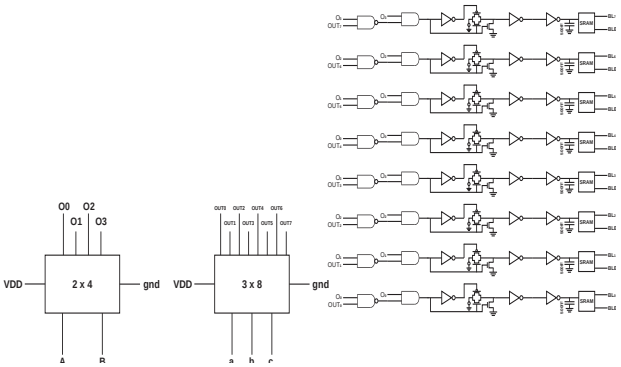

Figure 5: Block Diagram of Complete Pulse Decoder Circuit

III. Results and Discussions

The decoder is designed at 45nm technology using INVERTER, AND gate. For schematic design Cadence Virtuoso tool is used. For simulation Cadence Spectre is used. The pre decoder and post decoder circuitry are shown in figure 5.The post-decoder which is driven by the outputs of pre-decoder stage. Word lines are formed by post decoder. In figure 5, shows that one 2 to 4 and one 3 to 8 pre-decoder. 2 to 4 and 3 to 8 decoder generates the 4 and 8 outputs respectively. Each 8 outputs of 3 to 8 decoder are giving to as input to the 8 different NAND gates. Each 4 outputs of 2 to 4 decoder is fed to the first four NAND gates and same four outputs of 2 to 4 decoder is given to the next four NAND gates. All the eight outputs of eight NAND gates are given as input to the eight AND gates. These AND gates has two inputs one from the NAND gate and other one is output of the 2 to 4 decoder which is given earlier as input to the NAND gate. One pulsed signal is provided at the source to drain connection of transmission gate. This transmission gate passes the output when transmission gate is ON and corresponding word line of SRAM become active. By providing the pulse signal the active pulse is ON only for short period of total active clock period due to which power of the active circuit is reduces. In this paper analysis the output power of the circuit by varying the pulse width of TG which is provided at source to drain node. The varying period of TG signal is 35ns to 20ns.This circuit has one capacitance of 500f F and at the end it contain SRAM cell. The output of inverter before the Capacitance is used as input to word line of SRAM. Finally able to get the output at bit line and bit line bar.

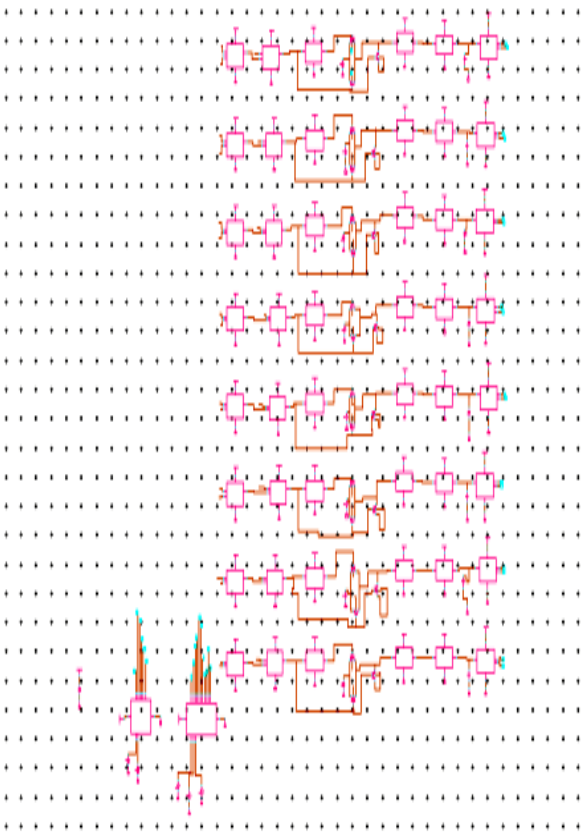

Figure 6: Schematic of Pulse Decoder Circuit

In this paper, we compare the existing decoder circuit with pulse decoder in terms of power. The old decoder design consist the two 2 to 4 decoder and one 3 to 8 decoder with transmission gate while pulse decoder consist one 2 to 4 and one 3 to 8 decoder , transmission gate with 6T SRAM and also consist the capacitance.

Table shows the comparisons of two different architectures in terms of power at voltage 1.1V.In which transmission gate pulsed signal is varied in terms of pulse width from range20ns to35ns.

Table I: Power Comparison of both the Decoder Architectures at Pulse Width 35 ns

	PULSE WIDTH(35)			
DECODER	Avg. power	Power y_{max}	Power y_{min}	Avg.leakage power
Optimized decoder	66.89uW	250uW	7.72uW	21.94uW
Pulse decoder	50.47uW	211uW	.0360uW	21.92uW

Table II: Power Comparison of both the Decoder Architectures a Pulse Width 30 ns

	PULSE WIDTH(30)			
DECODER	Avg. power	Power y_{max}	Power y_{min}	Avg.leakage power
Optimized decoder	64.12uW	342uW	1.54uW	21.92uW
Pulse decoder	45.36uW	220uW	.0215uW	21.92uW

Table III: Power Comparison of both the Decoder Architectures at Pulse Width 25 ns

	PULSE WIDTH(25)			
DECODER	Avg. power	Power y_{max}	Power y_{min}	Avg.leakage power
Optimized decoder	60.80uW	271uW	5.66uW	21.94uW
Pulse decoder	43.67uW	225uW	.0121uW	21.92uW

Table IV: Power Comparison of both the Decoder Architectures at Pulse Width 20 ns

	PULSE WIDTH(20)			
DECODER	Avg. power	Power y_{max}	Power y_{min}	Avg.leakage power
Optimized decoder	57.44uW	234uW	.155uW	21.94uW
Pulse decoder	43.21uW	256uW	0.0032uW	21.92uW

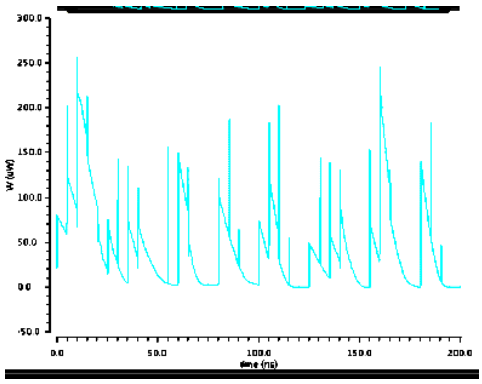

Figure 6: Transient Power Waveform at Pulse Width 35ns.

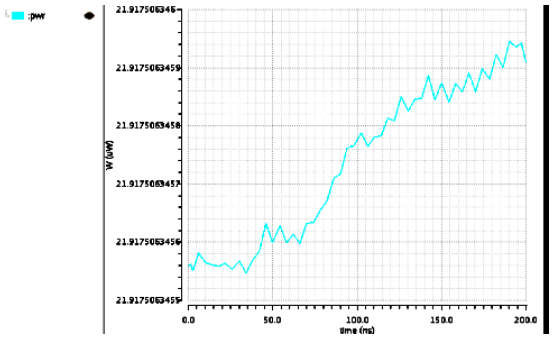

Figure 7: Transient Leakage Power of the Circuit at Pulse Width 35ns.

IV. CONCLUSION

This paper discussed about the access path of SRAM is divided into two portions one is row decoder other one is the data path. The power of the SRAM can be reduced by reducing the swings at the input signals. By controlling the pulse width of a transmission gate we are able to control the pulse width of word line due to which swings in voltages can be minimized. The row decoder is designed with the help of one 2 to 4 decoder and one 3 to 8 decoder at voltage 1.1V. This circuit transient average power is decreases as pulse width of transmission gate is reduced.

REFERENCES

[1] B.Amrutur and M. Horowitz, "Fast Low-Power Decoder for RAM". *IEEE J. Solid-State circuits*, vol.36 no.10, pp. 1506-1515,2001.

[2] Carlson S. Anderson, S. Natarajan, and A. Alvoandpour, " A high density, low leakage,5T SRAM for embedded Caches*". Proc. Of European Solid-State Circuit Conference*, pp.215-222,2004.

[3] Michael Powell, Se-Hyun Yang, Babak Falsafi, Kaushik Roy, and T. N. Vijay Kumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories". *in proceeding ACM, ISLPED,* koria,

[4] Liqiong Wei, Zhanping Chen, Kaushik Roy, Mark C. Johnson, Yibin Ye, and Vivek K. "Design and Optimization of Dual- Threshold Circuits for Low-Voltage Low-Powe Applications Transactions on very large scale integration system". *IEEE J. Solid-State circuits* , vol. 7 . no.1,1999.

[5] Bhatnagar Vipul, and Attri Chandani. "Optimization of row Decoder for 128x128 6T SRAM". *IEEE* Journal,2015.

[6] Shivkaran, Jain, Arun kr Chatterjee. "Nand gate architectures for memory decoder". *International* Journal Of Computers & Technology, pp. 610- 614, 2013.

[7] Michael A. Turi, and José G. Delgado-Frias. "High-Performance Low-Power Selective Precharge Schemes for Address Decoders". *IEEE Transactions On Circuits And Systems*, vol. 55,no.9,pp.917 – 921,2008.

[8] Yuan Ren, Gansen. M, and Noll. T. "Low power 6T-SRAM with tree address decoder using a new equalizer precharge scheme". *IEEE J. l solid state circuits.pp*.12-14,2008.