ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 4, April 2016

An Optimized Radix-8 Sum to Modified Booth Recoder for FAM Design

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***Abstract*—Complex arithmetic operations are widely used Digital Signal Processing(DSP)applications.This work focuses on implementation of one of complex arithmetic operations,the Fused Add-Multiply(FAM) operation.Two efficient radix-8 Sum to Modified Booth (S-MB) Recoding techniques are proposed in this work for FAM implementation.The FAM units incorpating the proposed radix-8 recoding technique shows significant improvement in terms of delay,area, power when compared with FAM units with already existing recoding techniques.**

Keywords—Add-Multiply operation,arithmetic circuits,Modified Booth Recoding,VLSI design.

I. INTRODUCTION

Digital Signal Processing is widely used in domains of multimedia,signalprocessing,etc.Most of these DSP applications carry out a large arithmetic operartions ,as their implementation is based of computationally intensive kernels like Fast Fourier Transform(FFT),Discrete Cosine Transform(DCT),etc.The performance of these DSP systems are greatly affected by decision regarding allocation and architecture of arithmetic units.

Recent research activities[3],[4] shows the improvements that can be achieved by common data sharing between different arithmetic units.In DSP applications like FIR filters often addition is followed by multiplication so instead of using two separate units an single dedicated unit can give better performance.This can be observed from Multiply-Accumulator(MAC) and Multiply-Add(MAD) units design in [5],[6].Apart from MAC/MAD operations many DSP applications are based on Add-Multiply operations like FFT algorithm in [12].

The direct design of AM unit requires the output of adder to be driven to input of multiplier.The use of separate adder and multiplier increases both area and critical delay.To minimize delay due to adder Carry Look Ahead(CLA) adder may be used but this increases area.Fusion techniques employed in [9]-[11], targeting optimized AM operators are based on direct recoding of sum of two numbers in its Modified Booth(MB) form[7].The use of constant time addition ensure that delay adder to be independent of input bit widths.In [9] the author proposes a two stage recoder which converts a number in carry save form to MB form.In [11] Zimmermann and Trans presented an improved design of [8] with less delay and area.The authorsDaumas and Matula in [10] presented an recoder that converts number in carry save form to borrow save form without changing critical path delay .

The existing recoding techniques may be efficient but perform complex manipulation at bit level.In [1] the authors proposed an Sum to Modified Booth(S-MB) recoder for implementing AM unit using Radix-4 algorithm.However in this work the number of partial product is reduced to half only.In [2] the authors proposed Radix-8 version of [1] using signed Full Adders alone resulting in partial product reduction by a factor of one by three.However the recoder in this work is made of Full Adders so area and delay of recoder increases.

In our proposed work the recoder unit is designed using Full Adder and signed Half Adders alone giving significant reduction in area and delay of AM unit when compared with [1],[2].Figs.1& 2 shows conventional AM unit and Fused Add-Multiply(FAM) unitrespectively.The Fused Add-Multiply design is implemented in structural Verilog HDL and functional verification is done using XILINX ISE 13.2. Synthesis is done using CADENCE RTL complier.

The rest of paper is organized as follows: In section II, recoding logic (a)redundant binary number system and (b)radix-8 Modified Booth multiplier is discussed.In section III,design of Radix-8 S-MB recoder and its implementation is dicussed.In section IV,Experimental analysis is given.In section V,summary is presented.

II. RECODING LOGIC

A. Redundant Binary Number System

A radix-r maximally redundant binary signed-digit number system has digits from set $D \in \{-\beta-1, \beta, ..0, ... \beta, \beta+1\}$where $r = 2^{\beta}$.The digit set D containingmore than two value gives multiplerepresentation for any binary number in signed digit format.An attractive property of redundant signed-digit number systemis that it allows carry-free addition as in in [8],[10].Addition can be carried out in constant time only if output is in redundant representation.The way redundancy

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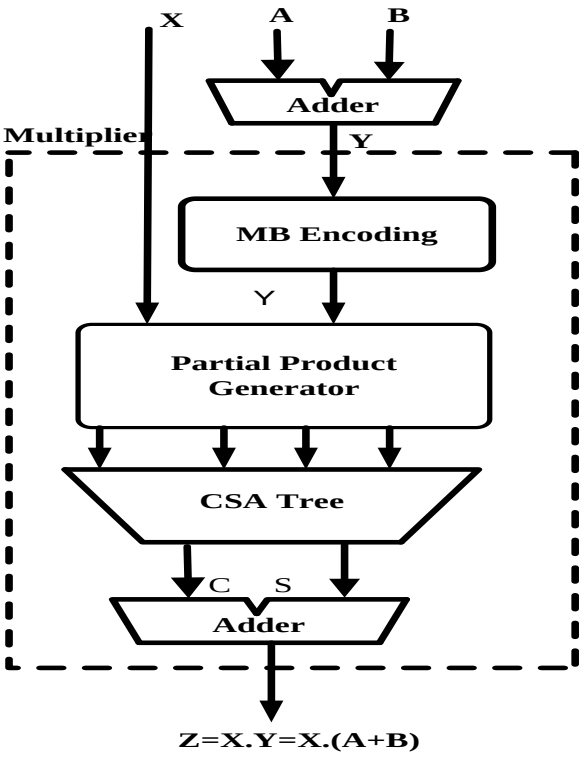


Fig. 1. Conventional Add-Multiply unit

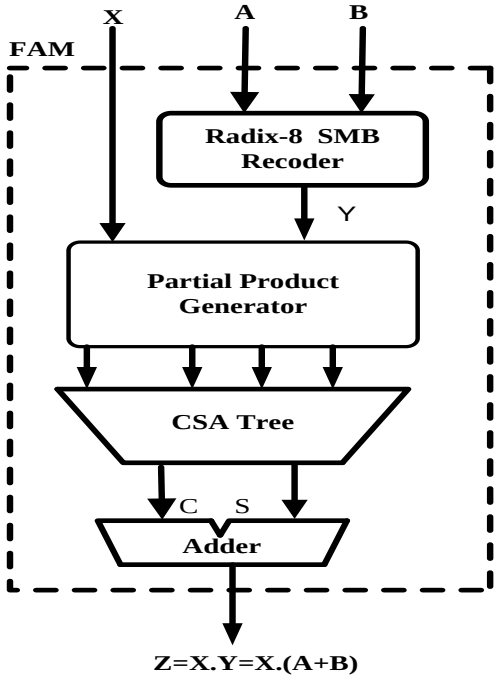


Fig. 2. Fused Add-Multiply unit

added greatly affect performance of constant time addition.Beginning from LSB of given number ,sum of each digit p_i is written in form as $s_i + 2 * t_i$ where s_i ,the interim sum is kept as it is while transfer digit t_i, is passed to next higher digit position.Adding interim sum and transfer digit yield a new digit and create no new transfer.Fig. 3 shows such an carry-free addition example .In [1] two bits are grouped but here three bits are grouped .Group size can be greater than three but this increases hardware complexity and increases delay.

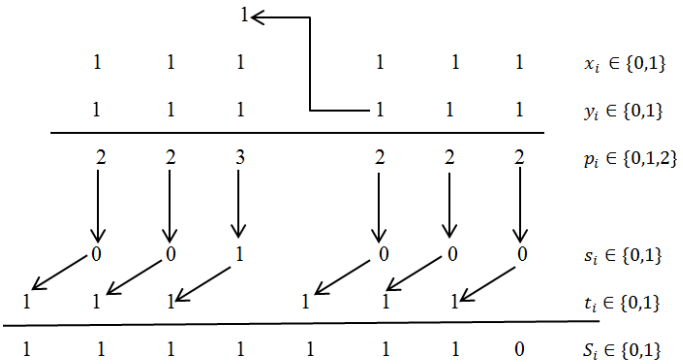


Fig. 3. Carry-free addition using redundant number system

The single stage carry propagation can be eliminated by simple look ahead scheme by computing sum S_i using $x_i, x_{i-1}, y_i, y_{i-1}$ directly.

B. Modified Booth Form

Modified Booth multiplier is an redundant signed digit radix-4 encoding technique .The main advantage of this multiplier is the number of partial product is reduced to half in multiplication.Radix-8 Modified Booth multiplier is a redundant signed digit radix-8 encoding technique where the number of partial product is reduced to n/3.This is a major advantage over radix-4 encoding scheme.

Consider multiplication of two numbers X and Y ,$n = 3k$ bits each.The multiplier Y can be expressed in MB form as:

$$Y = \langle y_{n-1}, y_{n-2}, \dots., y_1, y_0 \rangle = \sum 2^{3k} y_k^{MB} \quad (1)$$

where y_k^{MB} is an encoding of i[th] group,with encoding in the range $y_k^{MB} \in \{-4,-3,-2,-1,0,1,2,3,4\}$ .Each digit corresponds to four bits $y_{3k+2}, y_{3k+1}, y_{3k}, y_{3k-1}$ with one bit overlapped considering that y_{3i}=0.A radix-4 multiplier generates n/2 partial products while radix-8 generates n/4 partial products.So radix-8 multiplier produces fewer partial products when compared with radix-4 multiplier.This reduces adder in accumulation of partial products.

But in radix-8 multiplier there occurs a complexity when producing partial product 3X.This will generate extra delay .However this can be eliminated in FAM design since in most of applications like FFT often X is a coefficient term so 3X can be precomputed and can be fed directly into FAM unit. The MB digits are formed based upon following equation:

$$y_k^{MB} = y_{3k-1} + y_{3k} + 2y_{3k+1} - 4y_{3k+2} \quad (2)$$

The overlap is necessary to know about the operation occured in previous block since MSB of previous block act as sign bit.The encoding table given in Table II shows the operation to be done to compute partial product.

TABLE I.MODIFIED BOOTH ENCODING TABLE

y_{3k+2}	y_{3k+1}	y_{3k}	y_{3k-1}	y_k^{MB}
0	0	0	0	0
0	0	0	1	X
0	0	1	0	X
0	0	1	1	2X
0	1	0	0	2X
0	1	0	1	3X
0	1	1	0	3X
0	1	1	1	4X
1	0	0	0	-4X
1	0	0	1	-3X
1	0	1	0	-3X
1	0	1	1	-2X
1	1	0	0	-2X
1	1	0	1	-X
1	1	1	0	-X
1	1	1	1	0

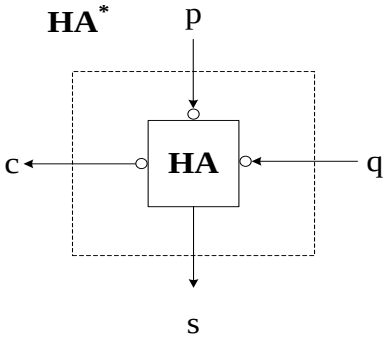
III. SUM TO MODIFIED BOOTH RECODING TECHNIQUE

A. *Design of Signed bit Half Adders*

In the design of radix-8 modified booth recoder [2],signed FAs implementing relation $2c_o - s = p - q + c_i$ and FAs implementing relation $2c_o + s = p + q + c_i$ have been used. Here to design Radix-8 Recoder,only signed bit HAs is used.More specifically,this Radix-8 Recoder is designed using two types of signed HAs referred as HA^* and HA^{**}.Tables II and III are their truth tables and Fig.3,4 shows their Boolean equation.Considering that p,q are binary inputs and c,s are outputsHA^* implements the relation $2.c - s = p + q$ where sum s is considered negatively signed (Table II,Fig. 3),the output take one of values {0,+1,+2}.HA^{**} implements relation $2.c - s = -p + q$ and produces output values {-1,0,+1}.

TABLE II. HA^* TRUTH TABLE

Inputs		Output Value	Outputs	
p(+)	*q(+)*		*c(+)*	*s(-)*
0	0	0	0	0
0	1	+1	1	1
1	0	+1	1	1
1	1	+2	1	0

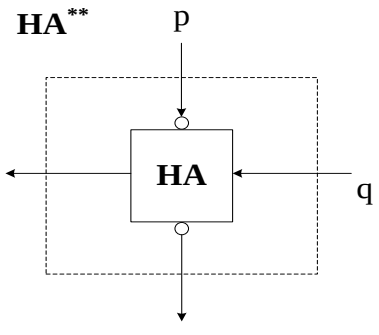


$$c = p \vee q$$
$$s = p \oplus q$$

Fig. 4. Boolean equation and schematics of HA^*

TABLE III. HA^{**} TRUTH TABLE

Inputs		Output Value	Outputs	
p(-)	*q(+)*		*c(+)*	*s(-)*
0	0	0	0	0
0	1	+1	1	1
1	0	-1	0	1
1	1	0	0	0



$$c = \overline{p} \wedge q$$
$$s = p \oplus q$$

Fig. 5. Boolean equation and schematics of HA^{**}

B. *PROPOSED S-MB RECODING TECHNIQUES*

In our proposed recording scheme signed HAs and normal FA areused to implement recoder.Inputs are in 2's complement format and input size of multiples of three are taken.

1) PR8T1 Recoding scheme:The first proposed scheme of Radix-8 recoding(PR8T1) is described in Fig.6.Assuming that inputs are in 2's complement form, starting from the LSB ,three consecutive bits of input A($a_{3k}, a_{3k+1}, a_{3k+2}$),B($b_{3k}, b_{3k+1}, b_{3k+2}$) are recoded into MB digit .From (2) we see that while forming MB digit the MSB is negatively weighted soHA^* and HA is used to form sum digit s_{4k+3} .The carry out $c_{4k+3,1}$ of $HA^*$is fed into next recoding cell FA as carry in.For k-1 recoding cell the HA is replaced by HA^*.The most significant digit (MSD) of this scheme is formed using the equation $y_k^{SD} = -c_{4k-1,1} + c_{4k-1,2}$.

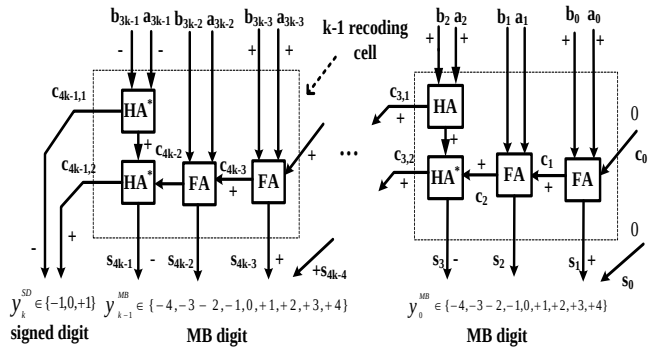


Fig. 6. PR8T1 recoding scheme

*2) PR8T2 Recoding scheme:*The second proposed scheme of Radix-8 recoding (PR8T2) is described in Fig. 7.In this scheme the MSB of each MB digit is formed using HA^{*} and HA^{**}.The carry out $c_{4k+3,1}$ of $HA^{*}$is fed into next recoding cell FA as carry in.For k-1 recoding cell the HA^{**} is replaced by HA^{*}.

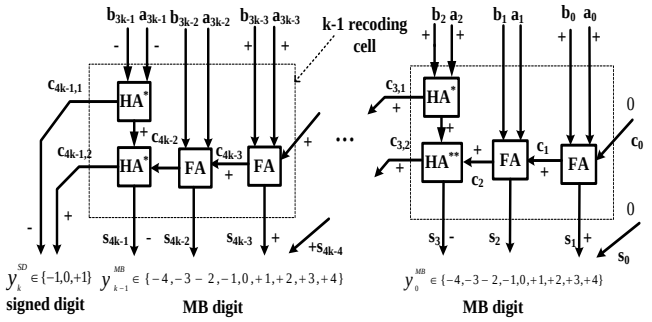


Fig. 7. PR8T2 recoder scheme

C. PARTIAL PRODUCT GENERATION:

Partial products are generated based on the radix-8 encoding scheme showed in Table I.2X is obtained by shifting X to left by one position and 4X by shifting X by two position.-2X,-4X are obtained by taking 2's complement of 2X,4X.3X is precomputed and directly fed into FAM unit.

D. ACCUMULATION OF PARTIAL PRODUCTS

Carry save adder(CSA) is used to sum partial products.The CSA is one of most efficient techniques to speed up digital designs that deal with multiple operand for addition and multiplication.ACSA reduces three operands into two operands without any carry propagation by saving the carry in next significant bit position.

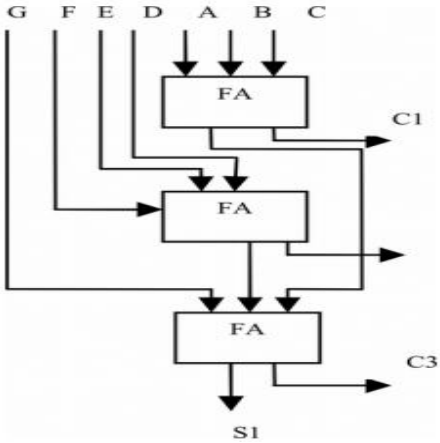


Fig. 8. Carry save adder adding six digits

IV. PERFORMANCE EVALUATION

To validate the performance the proposed schemes are compared with already existing scheme in [1],[2].For fair comparison the proposed and already existing recoders are included in 9,21,33 bit-width FAM designs.All the FAM design are implementeted using structural Verilog HDL and functional verification is done using XILINX ISE 13.2. Figs. 9-12 shows simulation waveform of proposed recoding techniques.

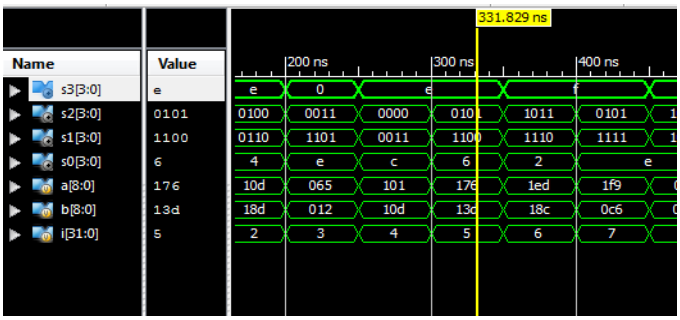


Fig. 9. Simulation waveform of PR8T1 MB recoder

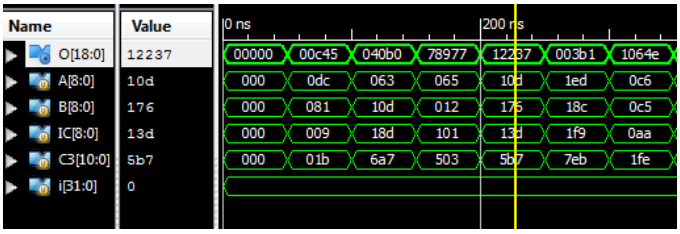


Fig. 10. Simulation waveform of FAM incorpating PR8T1 recoder

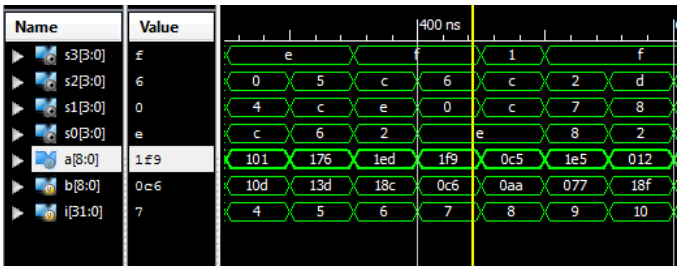


Fig. 11. Simulation waveform of PR8T2 MB recoder

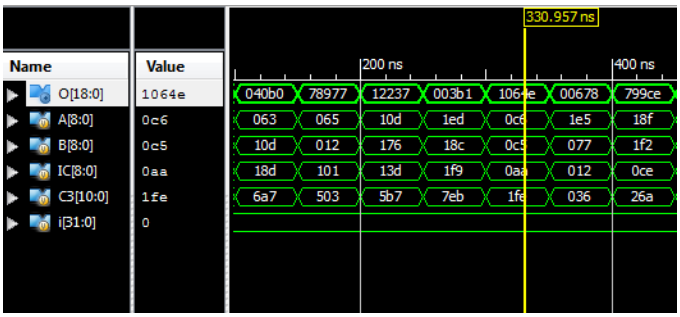


Fig. 12. Simulation waveform of FAM incorpating PR8T2 recoder

The FAM units incorpating proposed and already existing recoders are synthesized using TSMC 180nm standard cell library in CADENCE tool and power,area,delay are

measured.TablesIV-VI shows the measured area,power and delay.Figs. 13-15 present a comparison among all FAM designs in terms of area,power and delay.All values are normalized with respect to [2].

TABLE IV. AREA MEASUREMENT OF FAM DESIGNS

Area(μm^2)				
Work		*Bit-width*		
		9	21	33
[1]	R4T1	2110	9631	18893
	R4T2	2101	9629	18882
	R4T3	2118	9653	18927
[2]	R8T1	2067	9254	20883
PROPOSED	PR8T1	2059	9238	20874
	PR8T2	2067	9263	20902

TABLE V. DELAY MESUREMENT OF FAM DESIGNS

Delay(ns)				
Work		*Bit-width*		
		9	21	33
[1]	R4T1	4652	9162	13230
	R4T2	4720	9283	13111
	R4T3	4652	9162	13230
[2]	R8T1	4768	9249	13418
PROPOSED	PR8T1	4924	9227	13248
	PR8T2	4814	9276	13444

TABLE VI. POWER MEASUREMENT OF FAM DESIGNS

Power(µW)				
Work		*Bit-width*		
		9	21	33
[1]	R4T1	135.9	892.7	2188.3
	R4T2	133.3	896.8	2198.5
	R4T3	139.1	882.2	2222
[2]	R8T1	143.7	866.35	2267.5
PROPOSED	PR8T1	143.45	873.6	2257.9
	PR8T2	143.26	861.9	2272.5

A. *Area analysis*

From Fig. 13 we can see that the proposed PR8T1&PR8T2 show significant savings in terms of area for 9&21 bit FAM designs.When compared with [1] our proposed recoding techniques give upto 4% area savings.This area savings is due to the fact that number partial product gets reduced to n/3 in proposed radix-8 FAM when compared with n/2 partial products of radix-4 FAM design in [1].However for case of 33 bit FAM design there is an exception, this is because the area occupied by partial product generator in this case increases conteracting the savings achieved from partial product summing.

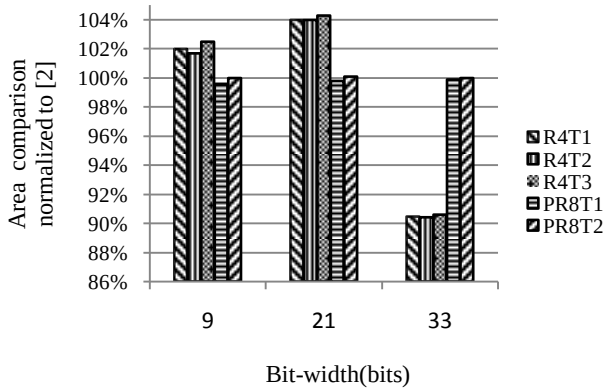


Fig. 13. Area comparison with all values normalized to the corresponding ones of [2]

When compared with [2] both PR8T1&PR8T2 show slightly improved area savings.Within the proposed techniques PR8T1 consume less area than PR8T2.

B. *Delay analysis*

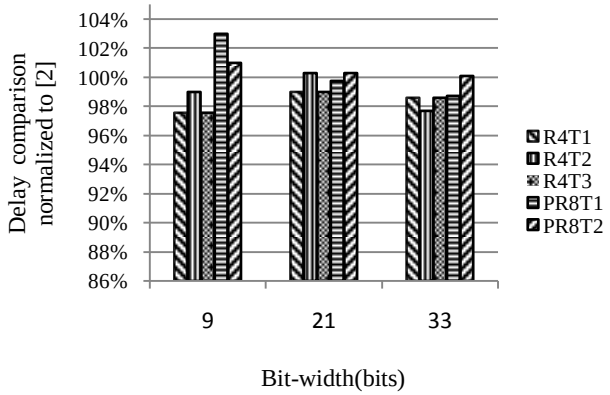


Fig. 14. Delay comparison with all values normalized to the corresponding ones of [2]

From Fig. 14 we see that when compared with [1] the delay of proposed techniques increases this is because of increased delay in recoder and partial product generator .However increase in delay is only upto 1% .Interestingly the proposed techniques give upto 1.5% reduced delay when compared with [2].

C. Power analysis

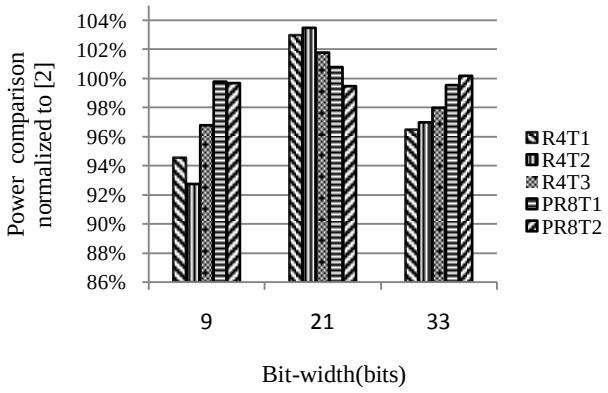


Fig. 15. Power comparison with all values normalized to corresponding ones of [2]

From Fig. 15 we see that for 21 bit FAM design the proposed techniques shows upto 3% reduction in power consumption.When compared with [2] , PR8T2 always give reduced power consumption.

V. CONCLUSION

This work focuses on optimizing the design of S-MB recoder for radix-8 Fused-Add Multiply(FAM) operator.It can be seen from Table IV FAM units incorpating the proposed recoder is area optimized upto to inputs of medium bit-width and power optimized for inputs of medium bit-width alone with a small tradeoff in delay.In future efficient implementation of partial product generator and its effects on performance need to be studied.

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