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Design And Implementation of Multiplier Using Reversible Logic In Multiple Accumulate Unit

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Abstract: **Reversible logic due to its reduced power consumption has captured substantial digital logic design. Its salient features are recovering from bit loss and unique input output mapping where conventional logic failed. The low power multiplier has been designed by using various reversible gates. The multiplier is designed and it is implemented in multiple accumulate unit, whereas the MAC unit consists of multiplier, adder and accumulator block. Here the multiplier multiplies the inputs and provides the result to the adder, which adds the multiplier result to the previously accumulated result. The adder block is designed using ripple carry adder and accumulated block is designed using D flip-flop whereas a clock pulse is required. All DSP's application uses MAC operation. The reversible gates such as Peres gate, Feynman gate and TSG gate are used. The parameters such as Area, Power, Delay are calculated. Then it is implemented in FPGA kit.**

***Keywords*— TSG gate, MFA gate, Peres gate. MAC, RC adder, D flip-flop**

I. INTRODUCTION

Energy dissipation is a vital contemplation in VLSI design. Reversible logic associates the energy with Landauer circumstances that information loss was predominantly due to utility irreversibility prominent to energy dissipation. Various logic gates and its applicability on logic design had been discussed by [Mamataj, Set all] extravagantly which finds its presentation in considerable calculating, low power CMOS, DNA calculating, digital signal processing (DSP), quantum dot cellular mechanisms etc.

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The loss of each information bit is KT × ln2 joules of energy, somewhere Boltzmann constant is denoted as K and T is the temperature at which the system is operative. In computing, especially digital signal processing, the multiply–accumulate process is a communal step that multiplies the product of two numbers and adds that product to an accumulator. The hardware unit that completes the process is well-known as a multiplier–accumulator (MAC, or MAC unit); the operation itself is also often called a MAC or a MAC operation. Modern computers may contain a realistic MAC, consisting of a multiplier applied in combinational logic shadowed by an adder and an accumulator register that supplies the result. The yield of the register is fed back to one input of the adder, so that on individually clock cycle, the output of the multiplier is further to the register. Combinational multipliers involve a huge amount of logic, but can calculate a product more rapidly than the method of shifting and adding typical of earlier computers. The first supercomputers to be furnished with MAC units were digital signal processors, but the method is now also mutual in general-purpose processors.

II RELATED WORKS

A.MAC Architecture

This segment defines four-bit reversible Multiply Accumulate Unit shown in number. A MAC unit is used to implement the multiplication and accumulator operations controlled to avoid redundant overhead on the processor in terms of processing time and the on-chip memory supplies. This is broadly used in Digital Signal Processing algorithms for high performance digital processing system. The projected reversible MAC unit includes of a four-bit reversible Multiplier, eight-bit reversible Adder and eight-bit reversible Accumulator register. The Multiplier multiplies the inputs and gives the result to the adder, which adds the multiplier result to the formerly accumulated result. The reversible Accumulator is intended using the reversible eight-bit register. The four-

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bit inputs X and Y are pragmatic to the multiplier unit which outcomes in eight-bit product. The product is applied to eight-bit adder unit which adds the earlier result kept in accumulator as well as the current out of the multiplier. Again the outcome of the adder is deposited back into the accumulator and this procedure will repeat till the previous bits.

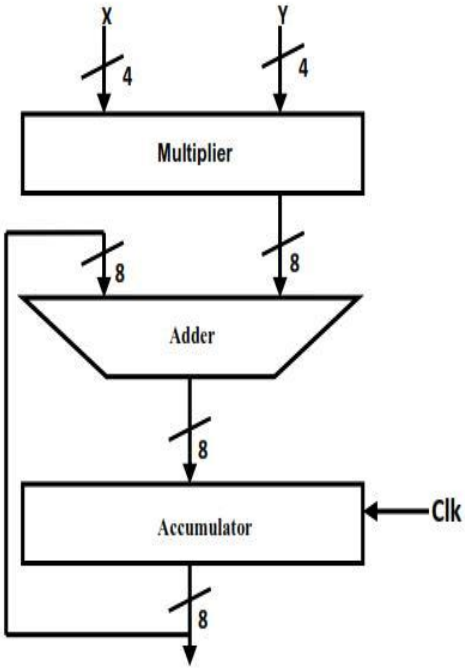

Figure 2.1 MAC Structure

In digital signal processing, Discrete Fourier Transform (DFT) calculation is most widely used where number of multiplications and additions should be achieved. Most of the power consumption arises during data manipulation. Therefore to reduce the power consumption DFT calculation can be executed by reversible MAC unit. The conventional multiply accumulate unit consists of multiplier and an accumulator register that comprises the sum of the preceding consecutive products.

The purpose of the multiply accumulate unit is specified by the ensuing expression Authority saving circuits are the requirement of the modern technology which can be there accomplished by using reversible logic. In this tabloid, we proposition an efficient design of a reversible n × n retained multiplier circuit, where n is the number of bits of each operand of the multiplier. We proposition a novel architecture of a general reversible compressor to reduce the number of partial products.

Two algorithms have been obtainable to hypothesis the Partial Product Generation (PPG) circuit and the Multi Operand Addition (MOA) circuit of the projected multiplier. Our projected design of MOA track only two steps to get the final output which is much augmented than existing Wallace Tree multiplier. During the recognition process of the multiplier, two new gates have been projected named as LS gate and LN gate to speed up the cluster of partial products. The capable study shows that our proposed design is much better than the prevailing approaches in terms of numbers of gates, garbage outputs, quantum cost and delay. This existing the design Methodology of an efficient and extensive reversible multiplier which everything for signed and unsigned binary numbers. The PPG and MOA circuits are grabbed by two algorithms which make the multiplication nearer by tumbling number of levels or steps. An estimate between existing and projected works has been offered in terms of diverse cost constraints to show the improvement of the predictable work. The replication verifies that our anticipated design works correctly. Our future reversible signed multiplier can be used in arithmetic logic unit which can be additional used to design a reversible processor for quantum computer.

B Adder

The adder we used here is ripple carry adder which is more exact and produce consistent results. Multiple full adder circuits can be dropped in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a reason in which the carry-out of each full adder is the carry in of the succeeding next most important full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs.

Proliferation stays privileged the logic circuitry is the motive behind this. Propagation delay is time intervened between the presentation of an input and existence of the corresponding output. Ruminate a NOT gate, When the input is “0” the output will be “1” and vice versa. The time taken for the NOT gate’s output to become “0” after the application of logic “1” to the NOT gate’s input is the propagation delay here.

Correspondingly the carry propagation delay is the time intervened between the suggestion of the carry in signal and the occurrence of the carry out (Cout) signal. Circuit

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diagram of a 4-bit ripple carry adder is shown below figured.

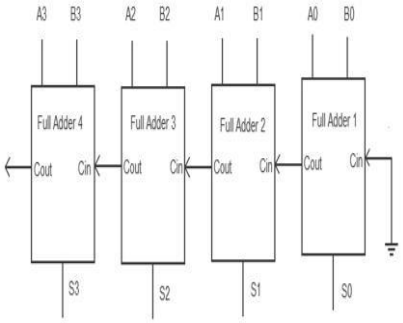

Figure 2.2 RCA

Sum out S0 and carry out Cout of the Full Adder 1 is operative only after the proliferation delay of Full Adder 1. In the comparable way, Sum out S3 of the Full Adder 4 is binding only after the joint proliferation intervals of Full Adder 1 to Full Adder 4. In humble words, the concluding outcome of the ripple carry adder is valid only after the joint proliferation delays of all full adder circuits inside it.

C. Accumulator

Accumulator is most widely used practical devices in digital systems. A register contains of a cluster of flip-flops combined together so that information bits can be stored in a digital system so that can be used later for computing process. Shift register is a register in which data can be shifted bit wise reliant on the clock signal. This section suggests Parallel-In-Parallel-Out (PIPO) shift register. The proposals uses the basic reversible gates considering the previous designs, we are aiming on sinking the quantum cost of each designs.

The D flip-flop is broadly used. It is also identified as a "data" or "delay" flip-flop. The D flip-flop captures the value of the D-input at a definite serving of the clock cycle (such as the rising edge of the clock). The caught value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line

D. Implementation of mac unit

For irreversible circuits, losing one bit of information dissipates (kTln2) joules of heat energy, where k is Boltzmann's constant and T is the absolute temperature. The reversible circuits do not dissolve energy as much as unalterable circuits. Thus, energy degeneracy is proportional to the number of bits lost during calculation. The reversible circuits do not lose information and can produce unique outputs from quantified inputs and vice versa (there is a one-to-one mapping between inputs and outputs). In order to accomplish low power designs Quantum computing and reversible circuits are used. In the minority of digital signal processing (DSP) claims the critical operations are the multiplication and Accumulation. Real-time signal processing necessitates high speed and high throughput Multiplier-Accumulator (MAC) unit that devours low power, which is always a key to realize a high performance digital signal Processing system. The main purpose of the proposed system is to design a MAC unit using reversible logic with least number of gates, number of garbage outputs, delay and quantum cost in order to prove it as an efficient design.

MAC unit is a simple arithmetic cell in computer handling units. Furthermore, reversible implementation of this unit is essential for quantum computers. Directing this purpose, various designs can be found. We calculated a novel 4x4 bit reversible multiplier circuit using Peres gates and HNG gates. That the planned reversible multiplier circuit is better than the existing designs in terms of hardware complexity, number of gates, garbage outputs and constant inputs. Furthermore, the restrictions of reversible circuits were highly avoided. The proposed reversible 4x4 multiplier circuit can be generalized for N x N bit multiplication. The prospect for further research includes the reversible implementation of more complex arithmetic circuits with less garbage outputs and low quantum cost.

E. Software Used

Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

Xilinx ISE is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for circuit synthesis and design.

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Cadence Design Systems, headquartered in San Jose, California, is a provider of electronic design skills and engineering amenities in the electronic design automation (EDA) industry. The corporation develops software charity to design chips and printed circuit boards, as well as intellectual properties (IP) casing a broad range of areas, includes interfaces, memory, analog, SoC peripherals, data plane processing units, and verification. The products of cadence include FPGA and ASIC design engineers, which are used to move a design into packaged silicon (ASIC), with products of custom and analog design, digital design, mixed-signal design, verification, and package/PCB design. To help integrate, verify, and implement complex digital SoCs, there are solutions that encompass design IP, timing analysis and signoff, services, and tools and methodologies. The company also provides products that assist with the development of complete hardware and software daises that support end applications.

III BASIC DEFINITIONS

Feynman gate is a 2*2 one complete reversible gate as exposed in figure 3.1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are demarcated by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate

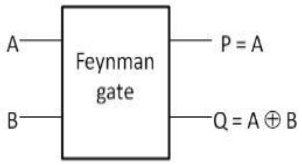

Figure 3.1 Feynman gate

Since a fan-out is not tolerable in reversible logic, this postern is useful for replication of the required outputs.

The 3*3 Toffoli gate which is publicised in the symbol 3.2 has the participation vector I (A, B, C) and the output vector is O(P,Q,R). The outputs are definite by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

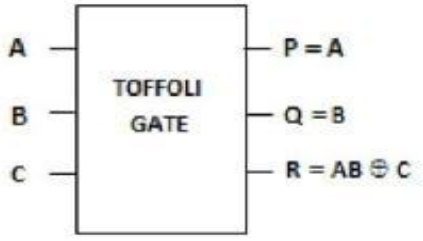

Figure 3.2 Toffoli gate

The 3*3 Fredkin gate which is pronounced in the symbol 3.3 has input vector I (A, B, C) and the output vector is O(P, Q, R). The output is demarcated by P=A, Q=A′B⊕AC and R=A′C⊕AB. Considerable total of a Fredkin gate is 5.

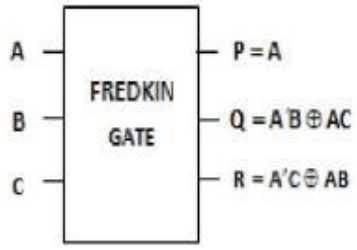

Figure 3.3 Fredkin gate

The 3*3 Peres gate has input vector I (A, B, C) and the output vector is O (P, Q, R). The output is demarcated by P = A, Q = A⊕B and R=AB⊕C. Quantum cost a Peres gate is 4. In the projected proposal Peres gate is charity because of its lowest quantum cost which is revealed in the numeral 3.4

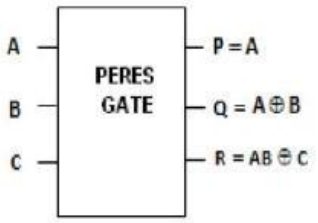

Figure 3.4 Peres gate

GARBAGE OUTPUTS

Annoying or unexploited output of a reversible gate (or circuit) is branded as garbage output, that is, the productivity(s) which is (are) required only to continue the reversibility is (are) known as garbage

productivity(s). Heavy price is paid off for each garbage output. The illustration for garbage outputs is given beneath where g1 and g2 are garbage harvests.

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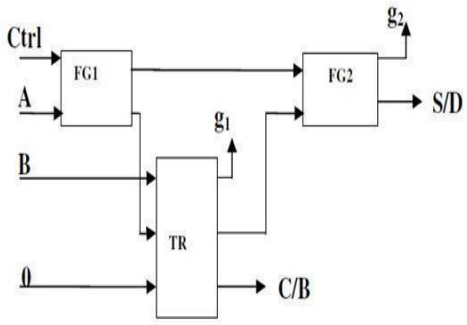

Figure 3.5 Garbage outputs

QUANTUM COST

The considerable rate can be consequential by replacing the reversible gates of a course by a cataract of uncomplicated quantum gates. Rudimentary quantum gates recognise quantum circuits that are innately reversible and deploy qubits rather than pure logic values. The state of a qubit for two uncorrupted logic states can be expressed as $|c\rangle = \alpha|0\rangle + \beta|1\rangle$, where $|0\rangle$ and $|1\rangle$ represent 0 and 1, respectively, and α and β are the complex numbers such that $|\alpha|2 + |\beta|2 = 1$. The most used uncomplicated quantum gates are the NOT gate (a single qubit is inverted), the CNOT gate (the target qubit is reversed if the single control qubit is 1), the controlled-V gate (also known as a square root of NOT, since two following V operations are equivalent to an inversion), and the controlled-V + gate (which performs the inverse operation of the V gate and thus is also a square root of NOT).

AREA

The extent of a logic journey is the addition of detached area of respectively gate of the circuit. If a reversible circuit consist of n reversible gates and the extent contains (a_1, a_2, ..., a_n). The area (A) of circuit is

$$= \Sigma(\ )_{=1} - - - - - (1)$$

The area of a circuit can be considered easily by locating extent of respectively distinct gate consuming CMOS 90nm Cadence Design Systems.

POWER

The supremacy of a logic course is the addition of detached power of each opening of the circuit. If a reversible course consist of n reversible gates and the power contains (p_1, p_2, ..., p_n). The extent (P) of track is

$$= \Sigma(p\ )_{=1} - - - - - (2)$$

The supremacy of a circuit can be measured easily by gaining power of each individual postern consuming CMOS 90nm Cadence Design Systems.

IV RESULTS AND DISCUSSION

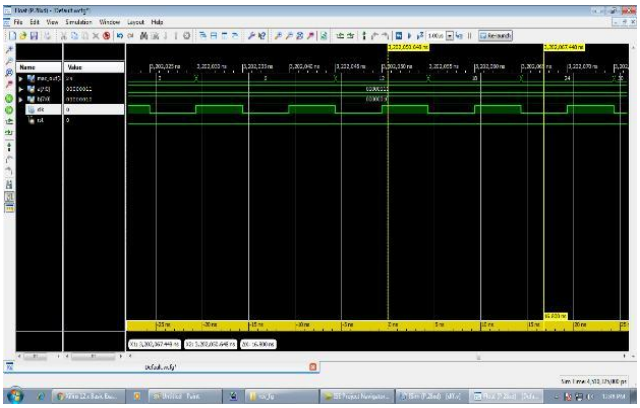

Figure 4.1 MAC FG

The output consist of 8 bit values both values are multiplied and the output is fed as input for adder and the corresponding output is produced which is given as input for accumulator whereas the accumulator and adder are combined together then final output is produced in the cyclic manner. This is shown in the figure 4.1.

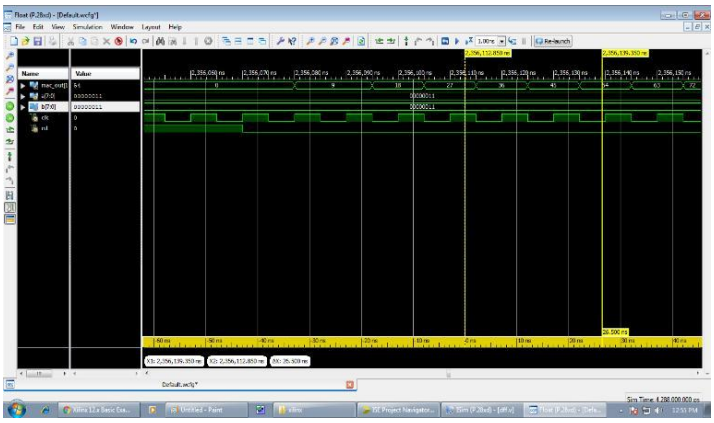

Figure 4.2 MAC TSG

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This illustrates the TSG gate output clock and reset signals are enabled which is shown in the figure 4.2. The mac output goes continuously as cyclic process such as 0,9,18,27,36,45,54 and so on.

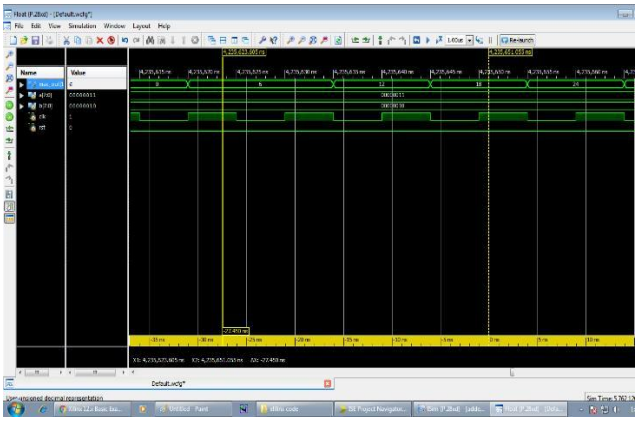

Figure 4.3 Mod_Mul

The output of multiplier is shown in the figure 4.3.

Performance Analysis

Gates used	Area	Power	Delay
FG	149	188mv	54.567ns
TSG	150	188mv	57.626ns
MOD_MUL	145	182mv	51.400ns

Table 4.1 performance metric

The performance analysis shows the various reversible gate parameters in table 4.1. By analysing these gates mod_mul consumes low power, area, delay. When compared to these reversible gates this mod_mul produces good results.

V CONCLUSIONS

The existing method consists of reversible multiplier concepts which include partial product generation and full adder. In the existing method Peres gate is used for both partial product generation and full adder. Therefore the proposed method consists of MAC unit which include multiplier, adder and accumulator. The clocked signal is used to control the output. The ripple carry adder is used to perform addition operation whereas it is more efficient when compared to other adders. The parameters also analysed such as area, power, delay, garbage output, quantum cost. Further it can be implemented using Field Programmable Gate Array kit.

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