ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 4, April 2016

Design And Performance Analysis of 6T SRAM cell at 90nm Technology

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***Abstract*— CMOS RAM Cell consumes very less power and requires very less read and write time. As the technology is improving channel length of MOSFET's are being scaled down, which causes stability of SRAM the major concern for future technology? A SRAM cell must meet channel length, stability and noise margin requirements for operation in submicron/nano ranges, therefore we have to modify conventional 6T SRAM circuit with additional circuitry and further different kind of parametric analysis can be done and functionality is verified using Micro wind for 90nm technology files.**

***Index Terms*— SRAM, Micro wind, 90nm Technology**

I. INTRODUCTION

Today SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory. Also, power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances Static Random access memory (SRAM) is an important functional element in most modern semiconductor products.

II. DESIGN OF CONVENTIONAL 6T SRAM CELL

The 6-T SRAM cell operates as follows:

1. For understanding read operation, the drive current of the pull-down transistor is such that of the pass-gate transistor should be sufficiently large. It is also known as cell Beta ratio. The bit-lines are pre-charged to a high level and then the word-line is selected. On the side of the cell storing a Logical "0", the bit line is discharged via the pass-gate transistor and pull-down transistor, so that a differential voltage develops between the bit-lines. This differential voltage must be large enough for a sense amplifier to detect the state of the cell. However, the differential voltage should not be too large, otherwise the cross-coupled inverters could flip their state and data stored might change.

2. For understanding write operation, the ratio of the drive current of the pass-gate transistor to that of the pull-up transistor should be sufficiently large. It is also known as cell gamma ratio. The bit-lines are driven to complementary voltage levels via a write driver and then the word-line is selected. On the side of the cell for which the bit-line voltage is logical "0" the internal storage node is discharged through the pass-gate transistor. The cross-coupled inverters raise the voltage on the opposite storage node and also latch the cell.

3. For understanding Standby Operation, the word line remains un-changed so that the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters formed by M1-M2, M3-M4 will continue to reinforce each other as long as they are connected to the supply to hold the previous data.

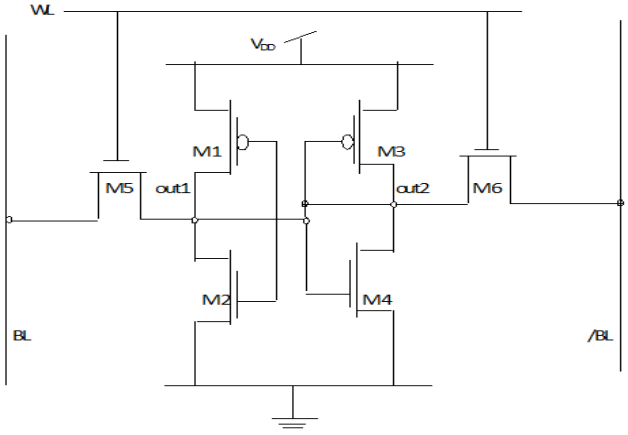

Fig.1 6T-cell schematic

In Conventional 6T SRAM Cell there are various limitations, as the voltage is scaled down to overcome the rise in power and other issues, e.g., the lower noise margins arises that can be controlled with some modification. During a read operation, the selected latch outputs transfers the stored value onto the two bit-lines. Since the bit-lines are always recharged, the bit-line differential voltage decreases. We can use sense amplifiers to improve the differential voltage from the bit lines. The sense amplifier to detect the voltage difference on the bit lines is shared by multiple bit lines and connection of the sense amplifier to a bit line pair is controlled by a column selection line. The main advantage in using a differential bit-line is common-mode rejection, which reduces noise effects and signal degradation. A cross-coupled amplifier is used for the sense amp. Once a memory cell is

Manuscript received April, 2016.
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selected for the read operation, the voltage on one of the complementary bit lines will start to drop slightly.

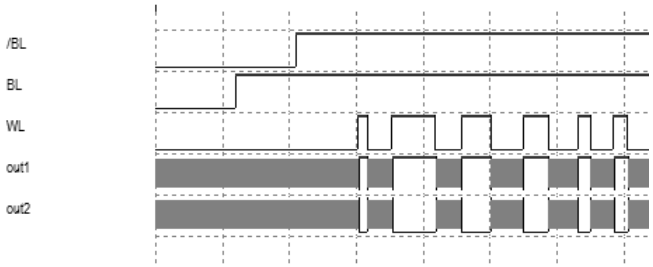

Fig.2 Timing Diagram of 6T cell

III. CMOS TECHNOLOGY USED

In this paper we are implementing SRAM technology being fabricated in 90 nm. The main key features of 90 nm technology in comparison to other technologies are:-

- Using standard transistors, these are 25% faster in gate level design.
- The densities of transistors are doubled.
- The area used by SRAM reduced by almost 50%.

IV. READ DELAY

Let us suppose that the content of the memory to be written is a 1, stored at node out1. The read cycle starts by firstly pre-charging both the bit lines to a logical 1, then secondly asserting WL high, that enables both the access transistors. The next step occurs when the values stored in nodes **out1 and out2** are transferred to the bit lines and leaving BL at its precharged value and discharging BL bar through transistors M6 and M4 to a logical 0. On the BL side, the transistors M5 and M1 pull the bit line toward VDD. If the content of the memory were a 0, the opposite would happen and BL would be pulled toward 1 and BL toward 0. Then these BL and BL-bar will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The more sensitive sense amplifier is, the faster is the speed of read operation of SRAM.

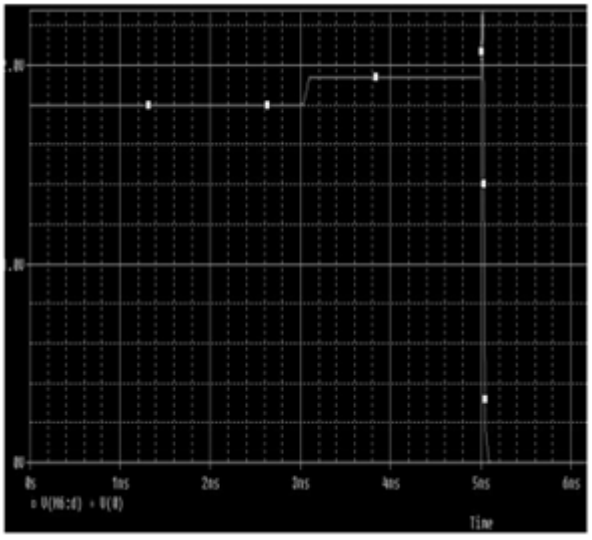

Fig. 3 Read Delay in 6T cell at 90nm

V. WRITE DELAY

Write cycle starts by applying the data to be written on bit lines. Let's say, if we want to write a 0, we must apply a 0 to the bit lines. After that WL is asserted high and the value that is to be stored is latched in. The bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful size of the transistors in an SRAM cell is required to ensure proper operation. As reference from the figure, transistors M5 and M6 are connected to write line and transistors M1, M2 and M3, M4 are connected to read line. Also these transistors are high voltage transistor.

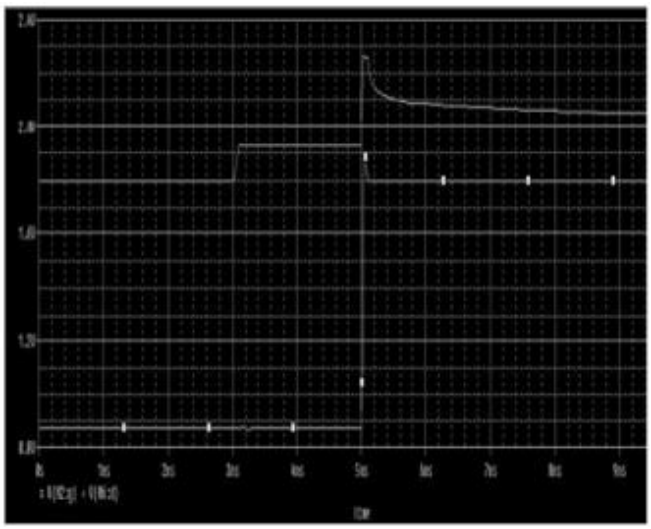

Fig. 4 Write Delay in 6T at 90nm

VI. POWER CONSUMPTION

The power consumption for 6T SRAM cell at 90nm and 180nm are compared below.

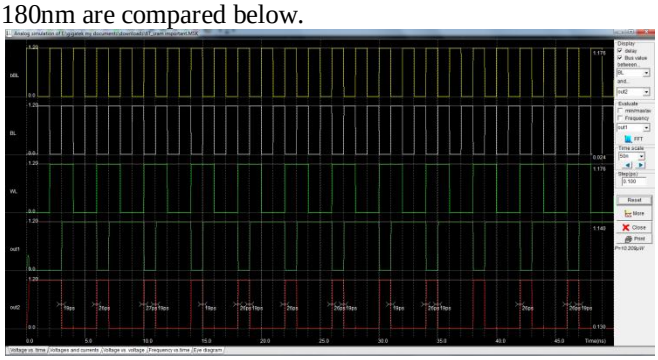

Fig 5 Power Dissipation in 6T @ 90nm

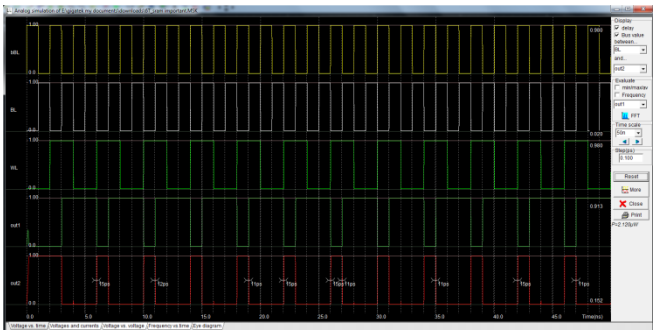

Fig 6 Power Dissipation in 6T @ 180nm

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
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VII. FREQUENCY OF OPERATION

Following are the figures for comparison of operating frequency of 6T cell at two different frequencies.

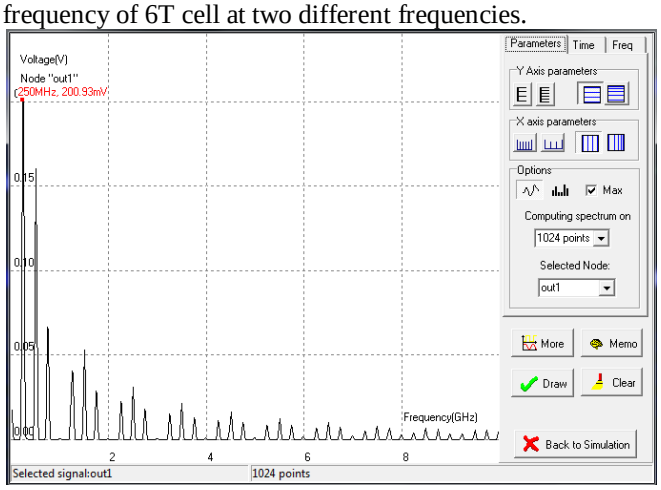

Fig 7 Frequency of operation for 6T @90nm

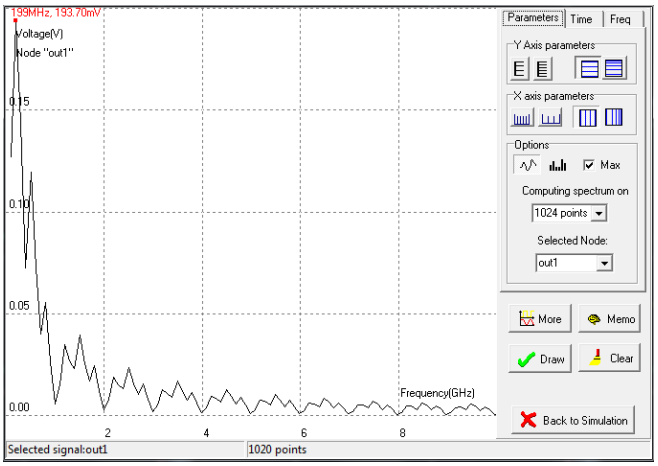

Fig 8 Frequency of operation for 6T @180nm

VIII. READ SIGNAL NOISE MARGIN

Following is the butterfly diagram for RSNM of 6T cell at 90nm technology. The curve is generated by plotting the input voltage vs. the output voltage of each inverter.

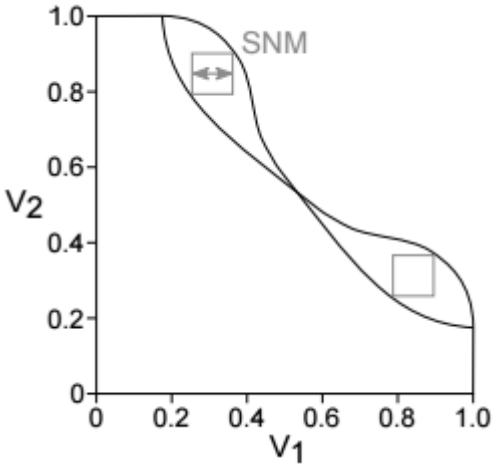

Fig 9 RSNM for 6T cell at 90nm

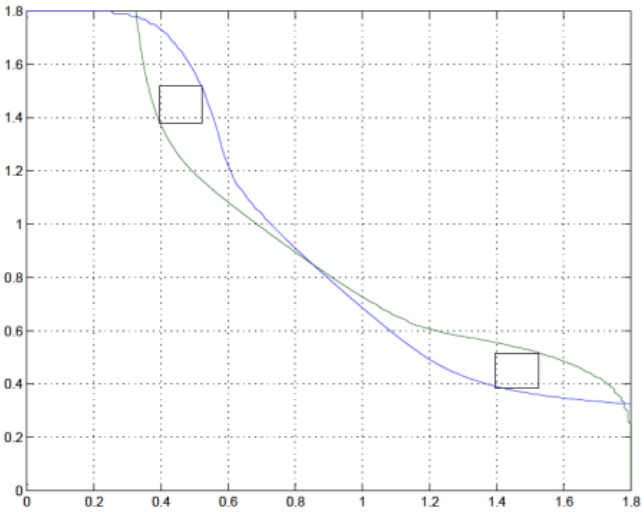

Fig 10 RSNM for 6T cell at 180nm

IX. WRITE SIGNAL NOISE MARGIN

Following curves are plotted for 6T cell in write operation and subsequent results are plotted and compared.

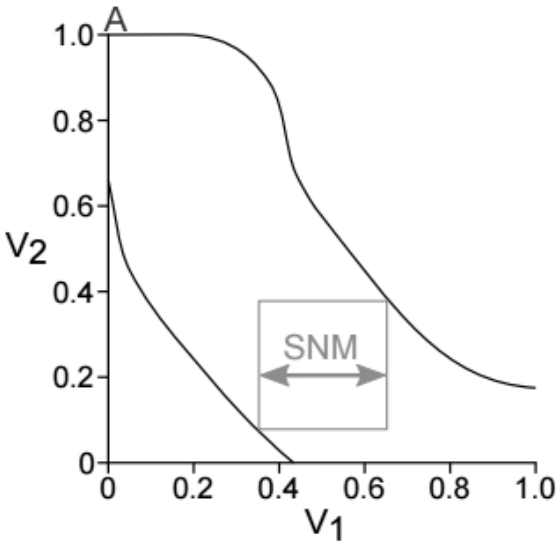

Fig 11 WSNM for 6T cell at 90nm

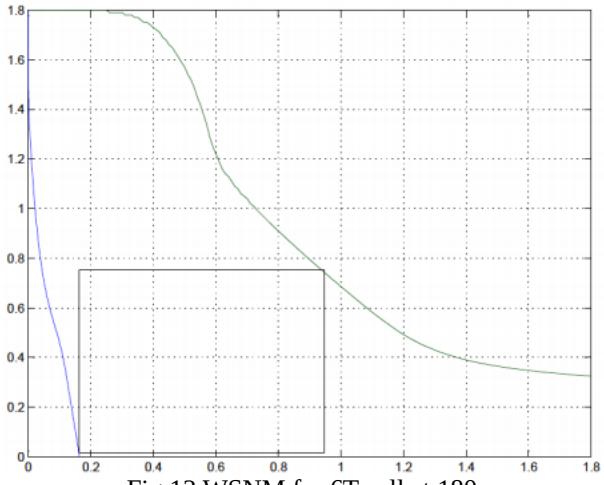

Fig 12 WSNM for 6T cell at 180nm

X. CONCLUSION

In this paper, performance analyses of 6T SRAM cell with following factors are analyzed. As technology goes sub micrometer delay affects the operation and same as supply voltage increase power dissipation also increase. The simulation results using Micro wind tool much better performance achieve using modified 6T SRAM cell with sense amplifier.

ACKNOWLEDGMENT

The author would like to thank SGT Institute of Engineering Technology, Haryana, India for providing the Tools and Technology for the work to be completed

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