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Single Phase Cuk Rectifier To Get Positive Output Voltage And Reduced Total Harmonic Distortion.

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Abstract— **A single-phase bridgeless Cuk ac/dc power factor correction (PFC) rectifier with positive output voltage is proposed in this paper. For low output voltage product applications, the rectifier is designed to convert high input voltage to low output voltage.The proposed rectifier operates in discontinuous conduction. A simple translation method to have the positive output voltage is the Cuk converter.The design,operation procedure of the proposed rectifier are addressed in detail in this paper. Simulation and experimental results obtained from a 150-W rated prototype circuit with input of 90–130 Vrms, 60 Hz, and output of 48 Vdc have verified the validity of the proposed rectifier.**

***Index Terms*—AC–DC power converter,Cuk, discontinuous conduction mode (DCM), positive output voltage, power factor correction (PFC), voltage control, zero-current switching (ZCS).**

I. INTRODUCTION

In recent years, switched-mode power supply technologies have rapidly developed. Most switched-mode power supplies for electronic products are used to convert ac to dc sources in different applications. The use of a transformer, a bridge rectifier, and capacitors can achieve a dc output voltage easily, but current at the input may be seriously distorted.

Therefore, PFC converters are critically required for ac–dc conversion[1] .Many circuit congfigurations have been developed for the PFC applications. The conventional PFC converter is a full-bridge rectifier, followed by a boost converter, as shown in Fig. 1. The converter is widely used because of its simplicity. However, due to boosting behavior of the converter, the output voltage is always greater than the input voltage.

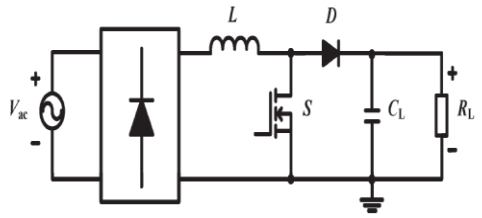

Fig. 1. Conventional boost PFC converter

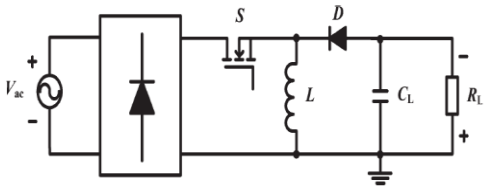

Fig. 2. Conventional buck–boost PFC converter.

The buck converter is seldom used in the PFC application, since, as the input current of the buck converter is discontinuous, it would lose control when the input line voltage is lower than the output voltage[2]. In addition, to filter the input current, additional passive filter must be used at the buck converter input. A buck PFC rectifier has been recently proposed in[3] for voltage step-down applications.

The buck PFC converter may lead to increased total harmonic distortion (THD) and reduced power factor (PF)[4] . Therefore, in such applications, converters such as Cuk converter are often used next to a full-bridge rectifier, as shown in Figs. 2–3,[5]-[13]to have a PFC converter with low output voltage.

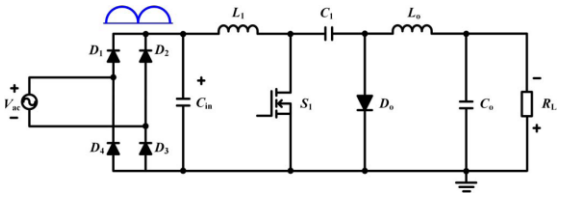

Fig. 3. Conventional Cuk PFC converter.

All the converters aforementioned can be used in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). While operating in DCM to shape the input current sinusoidally, these converters have intrinsic PFC characteristics at fixed duty ratio[14] , there is no need of any control circuit.However, the drawbacks of buck–boost converter operating in DCM are high-current stress on semiconductor devices and discontinuous input current, which increases the THD. On the other hand, Cuk converters are the ones whose input currents are continuous, while operating in DCM with the output voltage lower than the input voltage[15].

The Cuk converter has both continuous input and output currents with a low current ripple.Thus, for applications requiring low current ripples at both the input and output ports of the converter, the Cuk converter seems to be a better candidate in the basic converter topologies. In practical applications, the DCM operation of the Cuk converter significantly increases the conduction losses, due to the increased current stress on the circuit components. However, using CCM for low-power applications, it requires extra components to achieve PFC performance . As a result, additional circuit cost is increased. This limits the DCM operation of the Cuk converter only in low-power applications (< 300 W) .

In a conventional PFC Cuk rectifier, as shown in Fig. 3, the current flows through bridge diodes and the power switch (S_1) during the switch on-time and through bridge diodes and the output diode (D_o) during the switch off-time. Thus, during each switching cycle, the current flows through three power semiconductor devices. As a result, the significant conduction loss caused by the forward voltage drop across the bridge diodes degrades the converter's efficiency, particularly at low line input voltage. To reduce the conduction losses, the number of semiconductor devices should be reduced in the current path. Some methods to reduce conduction losses in Cuk are proposed but the Cuk converter has negative output voltage. Therefore, the extra requirement is an inverse amplifier circuit to translate the negative into the positive voltage[20].The additional inverse amplifier circuit thus increases the cost.

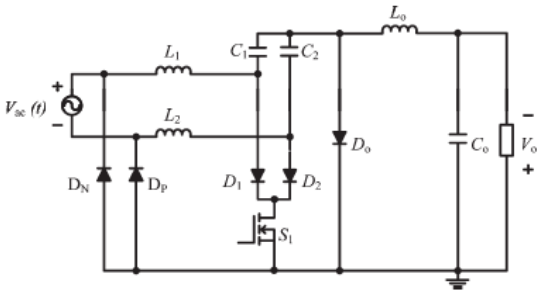

Fig. 4. Proposed bridgeless Cuk PFC rectifier with negative output voltage.

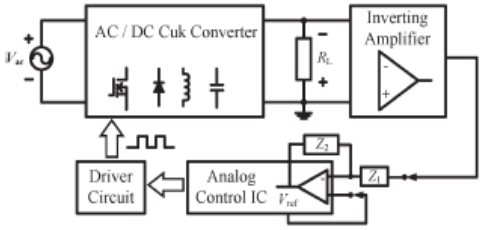

Fig. 5. Blocking diagram of the conventional Cuk PFC circuit (with negative output voltage).

II. Proposed Bridgeless Cuk PFC Rectifier With Positive Output Voltage

Fig. 4 shows the proposed initial bridgeless Cuk PFC rectifier, which has a negative output voltage, like the existing Cuk PFC rectifier. As noted, for this circuit, an inverting circuit to transfer the negative to the positive output voltage is still required for analog feedback control, as shown in Fig. 5. To obtain the positive output voltage without the inverting amplifier circuit, it is possible to transfer the polarity of all the components in Fig. 4 in the way as shown in Fig. 6, and obtain the proposed bridgeless Cuk PFC rectifier in Fig. 7. Thus, the feedback control circuit is simpler, and the cost can be also reduced, as compared with the conventional feedback control circuit shown in Fig. 5, although the power switch employed in the proposed circuit is floated with a high-side gate driver needed.

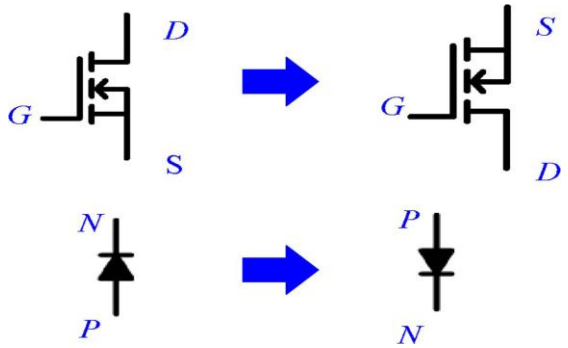

Fig. 6. Transferring the polarity of all components in the proposed initial topology in Fig. 4.

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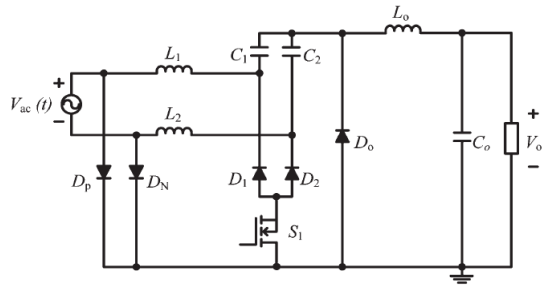

Fig. 7. Proposed bridgeless Cuk PFC rectifier with positive output voltage.

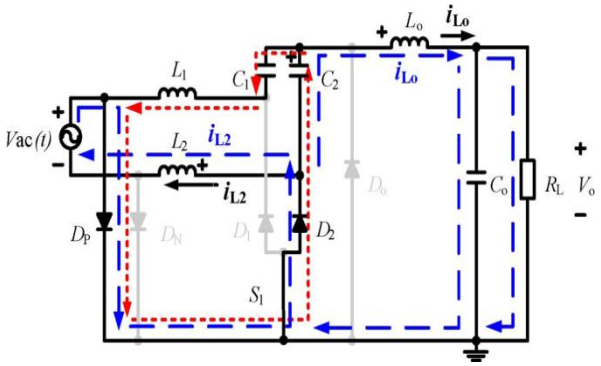

Fig. 8. Equivalent circuit in mode I (switch S1 is turned on).

A. PRINCIPLES OF OPERATION

Mode I [$t_0 - t_1$]: This mode starts when switch S_1 is turned on, as shown in Figs. 8 and 9. Input inductor L_2 starts to charge linearly in slope of $V_{ac}(t)/L_2$, and diode D_p is forward biased by the inductor current i_{L2}. The voltage across L_o is equal to $V_{ac}(t)$; thus, i_{Lo} increases linearly in slope of $V_{ac}(t)/L_o$. The inductor currents during this mode are given by

$$\frac{di_{Ln}}{dt} = \frac{V_{ac}(t)}{L_n}, \qquad n = 2, o. \quad (1)$$

Accordingly, the peak current through the active switch $S1$ is given by

$$I_{S1,\mathrm{pk}} = \frac{V_m}{L_e} D_1 T_s \quad (2)$$

—

where V_m is the amplitude of the input voltage $V_{ac}(t)$, D_1 is the switch duty cycle, and L_e is the parallel combination of inductors L_1, L_2, and L_o.

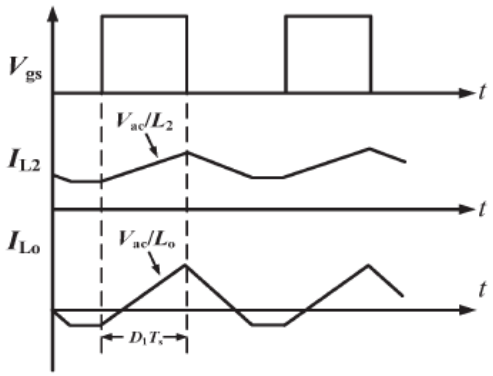

Fig. 9. Theoretical DCM waveforms during one switching period Ts in mode I (switch $S1$ is turned on).

Mode II [$t_1 - t_2$]: This mode starts when switch S_1 is turned off and diode D_o is turned on, simultaneously, as shown in Figs. 10 and 11. Input inductor L_2 starts to discharge linearly.

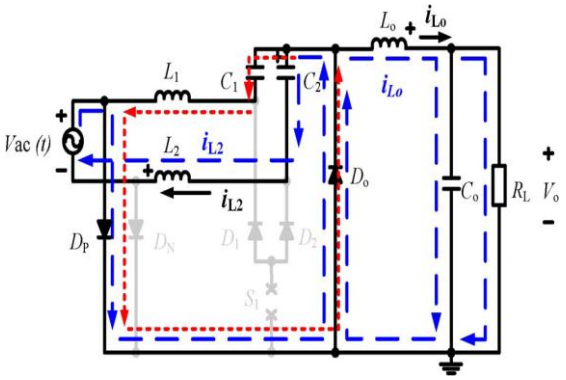

Fig. 10. Equivalent circuit in mode II (switch $S1$ is turned off).

in slope of $V_{ac}(t)/L_2$, and diode D_p is forward biased by the inductor current i_{L2}. The voltage across L_o is equal to V_o; thus, i_{Lo} decreases linearly in slope of V_o/L_o. Note that diode D_o is turned off at zero current. The inductor currents of L_2 and L_o during this mode are given by

$$\frac{di_{L2}}{dt} = \frac{-V_{\mathrm{ac}}(t)}{L_2}$$

$$\frac{di_{Lo}}{dt} = \frac{-V_o}{L_o}. \quad (3) \ \& \ (4)$$

Mode III [$t_2 - t_3$]: During this interval, only diode D_p conducts to provide a path for i_{L2}, as shown in Fig. 12.Accordingly, the inductors L_2 and L_o in this interval behave as constant current source. Thus, the voltage of inductors (L_2 and L_o) is zero. Capacitor C_2 is being charged by the inductor current i_{L2}, and the energy of capacitor C_o is released to load. This is a freewheeling mode. The theoretical waveforms in this mode are shown in Fig. 13.This mode lasts until the start of a new switching period. The turn-off time of the switch and the output diode is given by

$$toff = Ts - ton - tdon \quad (5)$$

where ton is the conducting interval of switch S1, and tdon is that of the output diode Do.
According to above equatiuons the normalized length of mode II period can be obtained as follows:

$$D_2 = \frac{D_1}{M}\sin\omega t \quad (6)$$

where ω is the line angular frequency, and M is the voltage conversion ratio (M = Vo/Vm).

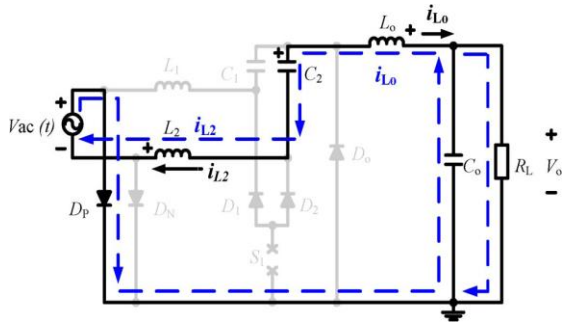

Fig11. Equivalent circuit in mode III (switch S1 is turned off).

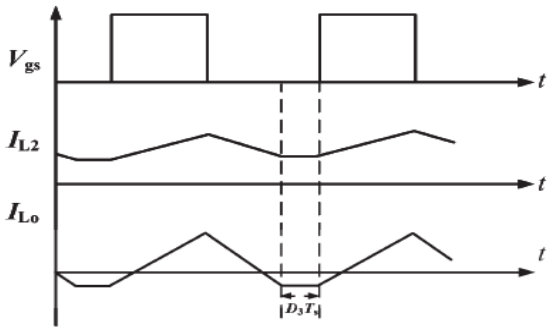

Fig. 12. Theoretical DCM waveforms during one switching period Ts in mode III (switch S1 is turned off).

B. ANALYSIS AND DESIGN OF THE PROPOSED CUK PFC RECTIFIER

1) Design of Input Inductors: According to the relationship of input current ripple ΔIL2, is in Figure7, and input voltage Vac in positive half cycle, the values of input inductor (L1 and L2) can be obtained as follows:

$$L_2 = \frac{V_{\rm ac}(t)D_1}{\Delta I_{L2} f_s}. \quad (7)$$

2) Voltage Conversion Ratio M: The voltage conversion ratio M can be obtained by applying the power balance principle as follows

$$P_{\rm in}(t) = \frac{2}{\rm T}\int_0^{\frac{\rm T}{2}} V_{\rm in}(t) I_{\rm in}(t)dt. \quad (8)$$

According to the large-signal model of the DCM switch network, it is noted that the average input current can be given as follows.

$$I_{\rm in}(t) = \frac{V_{\rm in}(t)}{R_{\rm in}} \quad (9)$$

where *R*in is defined as the input resistance and given by

$$R_{\rm in} = \frac{2L_e}{D_1^2 T_s}. \quad (10)$$

Evaluating above equations the voltage conversion ratio can be given by

$$M = \frac{V_o}{V_m} = \sqrt{\frac{R_L}{2R_{\rm in}}}. \quad (11)$$

3) Boundaries Between CCM and DCM: To operate in DCM, the following inequality must be satisfied:

$$D2 \le 1 - D1. \quad (12)$$

By using above equations following condition for DCM is obtained:

$$K_e \le K_{e\_\rm crit} = \frac{1}{2(M + \sin(\omega t))^2} \quad (13)$$

where the parameter Ke is expressed as follows

$$K_e = \frac{2L_e}{R_L T_s}. \quad (14)$$

It is obvious that,the value of Ke_crit depends on the line angle ωt. Thus, the parameters of Ke_crit can be respectively obtained as

$$K_{e\_\rm crit(min)} = \frac{1}{2(M+1)^2}$$
$$K_{e\_\rm crit(max)} = \frac{1}{2M^2}. \quad (15)\&(16)$$

Therefore, for Ke < Kecrit(min), the proposed bridgeless Cuk PFC rectifier with positive output voltage always operates in DCM.

4) Selection of Input Capacitors: In the Cuk converter as PFC, voltages of the input capacitors C1 and C2 should be nearly constant value within the switching period Ts and follow the input voltage profile within a line period. In addition, the input capacitors C1 and C2 should not cause low-frequency oscillations with the converter inductors. Thus, the energy transfer capacitors C1 and C2 are determined based on

inductors L1,L2, and Lo values such that the line frequency fL should be well below the switching frequency fs. In addition, a better initial approximation for choosing the resonant frequency fr is given by

fL <fr < fs

$$f_r = \frac{1}{2\pi\sqrt{C_1(L_1 + L_o)}}. \quad (17)$$

5) Design of Output Capacitor Co: The output ripple frequency of the converter is two times of the input frequency.In the worst case, the output current during the half period of ripple frequency is provided by the output capacitor. Therefore, Co can be obtained as follows:

$$C_o = \frac{P_o}{4 f_L V_o \Delta V_o}. \quad (18)$$

6) Stresses on Semiconductor Devices: According to Figure10, the following expressions about the stresses on semiconductor devices as functions of input/output voltages and currents on inductors.

$$V_{D,\max} = V_{sw,\max} = V_{ac,\max} + V_o$$

$$I_{D,\max} = I_{sw,\max} = I_{ac,\max} + \Delta I_L - I_{L2,\min} \quad (19)\&(20)$$

where VD,max and ID,max are the maximum voltage and current stresses on diodes Dp, Ds, D1, D2, and Do; Vsw,max and Isw,max are the maximum voltage and current stresses on switch S1, respectively. Vac,max and Iac,max are the maximum input voltage and current, respectively; ΔIL is the current ripple of L1 or L2 and IL2,min is the minimum current of L2.

III. EXPERIMENTAL RESULTS

By following the specifications given in Table I and the design procedure described earlier, components and parameters used in the proposed power stage circuit are listed in Table II for verification of the proposed rectifier. Fig. 16 shows the experimental setup photograph of the proposed converter.

TABLE I
SPECIFICATIONS OF THE PROPOSED RECTIFIER

Specifications	
Input Voltage V_{in}	90-130 V_{rms}
Output Voltage V_{out}	48 V_{dc}
Rated Power P_{out}	150 W
Switching Frequency f_s	100 kHz

TABLE II
COMPONENT PARAMETERS USED IN THE PROPOSED CIRCUIT

Items	Proposed Circuit
Input Voltage V_{in}	90~130 V_{rms}
Output Voltage V_o	48 V_{DC}
Rated Power P_o	150 W
Switching Frequency f_s	100 kHz
Input Capacitors C_1 and C_2	1 μF
Output Capacitor C_o	2 mF
Input Inductor L_1 and L_2	1 mH
Output Inductor Lo	22 μH

The following figures shows the input, output voltages, capacitor C1 & C2 voltages, input current, duty cycle waveforms for the circuit proposed.

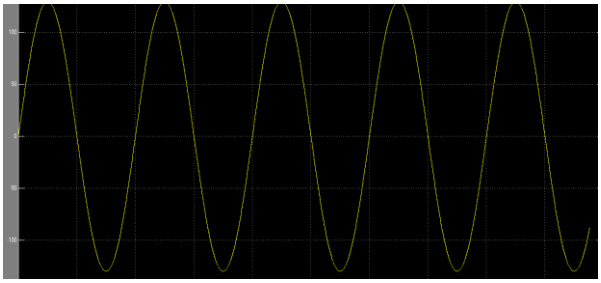

Fig 13.Input voltage waveform

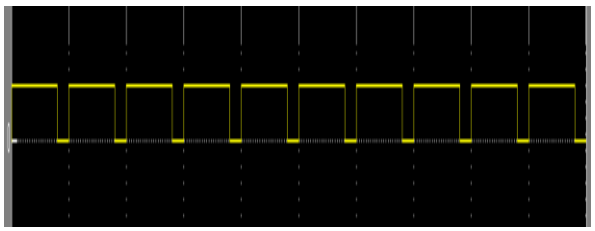

Fig 14.Duty cycle waveform

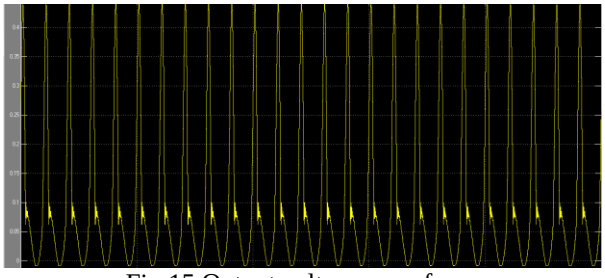

Fig 15.Output voltage waveform

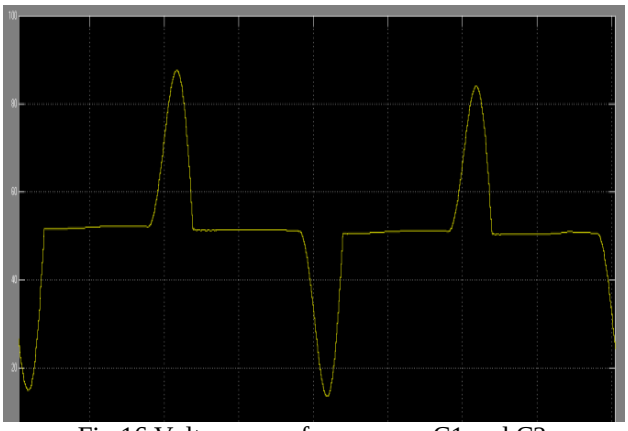

Fig 16.Voltage waveform across C1 and C2

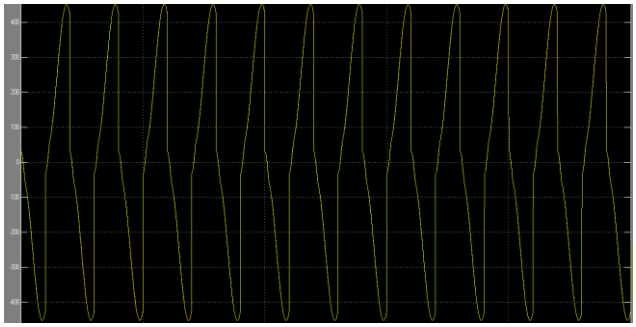

Fig 17.Input current waveform

TABLE III
CUK CONVERTER SIMULATION RESULTS

%LOAD	%THD	POWER FACTOR	VOUT
100	2.49	0.9961	48
90	2.76	0.9958	43
80	2.78	0.9506	38
70	2.85	0.993	33
60	2.9	0.9923	28
50	3.04	0.9918	24
40	4.5	0.9912	19
30	6.27	0.991	15
20	7.66	0.9908	10
10	7.8	0.98	5

IV. CONCLUSION

In this paper, the Cuk PFC rectifier with positive output voltage has been proposed and experimentally verified. The experimental results have shown good agreements with the predicted waveforms analyzed in the paper. The PF of the circuit has 0.99 above at all the specified input and output conditions.In addition, with only a single switch employed, the implemented system controla circuit is simple to achieve high PF by applying any pulsewidth modulation control integrated circuit. Moreover, as required in the traditional Cuk circuit, transferring the original negative output voltage to the positive one is not needed in the proposed Cuk topology.Convenience of using the Cuk rectifier can be thus obtained.

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