ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 6, June 2016

Improved Voltage Differencing Inverting Buffered Amplifier (VDIBA)

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***Abstract*—This paper presents Low Voltage Cascode Current Mirror (LVCCM) based low-voltage low-power variant of recently proposed an active element namely Voltage Differencing Inverting Buffered Amplifier (VDIBA). The proposed configuration operates at lower supply voltage 0.7 V with the total quiescent power consumption of 3.99mW at the biasing current of 100 uA. The simulations are performed using CADENCE 180 nm CMOS technology parameters with 0.7 V supply voltage to validate the effectiveness of the proposed circuit.**

***Index Terms*—Low Voltage , VDIBA, Low Power ,Analog Circuit Design.**

I. Introduction

As the technology is scaling and demand of portable electronic equipmentsis growing day by day , it has motivated the researchers in developing low-voltage low-power analog signal processing circuits. Low-voltage low-power design involves various promising techniques so that the complete analog circuit could meet the proposed design requirements. Various low-voltage, low-power design techniques have been reported in many literatures explaining techniquies like sub-threshold MOSFETs, level shifter approach ,self cascade approach, bulkdriven approach and use of FGMOS instead of simple MOSFETs [2–11].Blolek et al. [14] have introduced and explains behavioral model of new active element like Voltage Differencing Buffered Amplifier (VDBA),Voltage Differencing Current Conveyor (VDCC) Voltage Differencing Transconductance Amplifier (VDTA),. These active elements are obtained by replacement of current differencing unit in Current Differencing Buffered Amplifier (CDBA), Current Differencing Transconductance Amplifier (CDTA) etc. by the voltage differencing unit. The differential OTA at the input stage is used to generate the voltage difference in these newly introduced active elements. Theseabove suggested topologies have simpler structure as well as increased electronic tunability. Recently, Nobert Herencsar et al. [1] have introduced to an active element VDIBA that has gained wide popularity due to its simpler structure consisting only six MOS transistors. The input stage and the output stage of VDIBA consistsof operational transcoductance amplifier and unity gain inverting buffer respectively. Tunability feature of built-in OTA in these blocks is helpful for compensating the unwanted parameter variation caused because of PVT variations. though these modifications are attention-grabbing and give advantage of advanced electronic management, they lack the characteristics of low voltage and low power active component. Therefore, the major aim of this paper is to

introduce low-voltage low-power variant of typical VDIBA developed by integrating LVCCM that may well be utilized in more difficult applications.

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The paper is organized as follows: basics of LVCCM is given in Section II. New low-voltage low-power and high operating frequency variants of VDIBA are introduced and analyzed in Section III. Section IV deals with the simulation results and finally the paper is concluded in Section V.

II. LVCCM

Current mirror is one of the main building block of analog circuit coming up with that is employed for copying a current from one active device by controlling the current in another active device of a circuit, keeping the output current constant despite loading. The responsibilities of Current Mirror circuit are current amplification and to supply correct biasing to analog circuits.

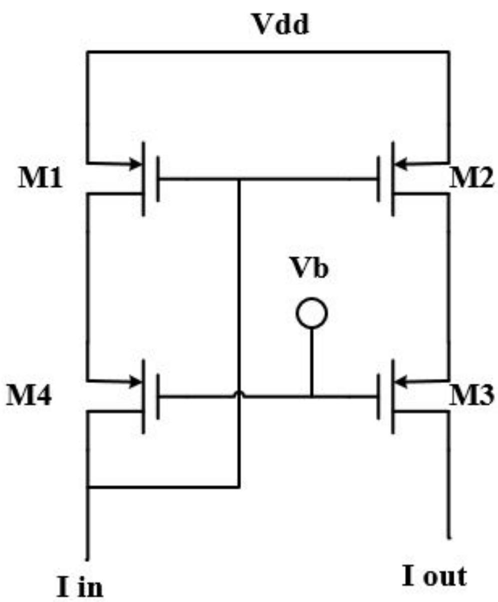

Fig.1: Low Voltage Cascode Current Mirror equivalent circuit

LVCCM aims to produce results at a lower operative voltage providing high output resistance than the simple current mirror because of the cascade configuration of the mirror .The equivalent circuit of LVCCM is shown in Fig.1. M1,M2,M3 and M4 are the pMOS transistors such that the gates of M3 and M4 operates by a controlled gate voltage known as biasing voltage of LVCCM denoted by Vb.

III. PROPOSED LOW-VOLTAGE LOW-POWER LVCCM BASED VDIBA

CMOS implementation and equivalent circuit symbol of standard VDIBA [21] is shown in Fig. 2 and 3 respectively. The input stage of VDIBA consisting transistors M1-M4 makes the OTA stage that converts the differential input voltage into current. The output stage fashioned by M5-M6 is a unity gain inverting buffer with M5 operating as nMOS load. The circuit has highimpedance input ports of OTA i.ep and n, a high impedance output port z and a lower impedance outputvoltage port w. Port relations of VDIBA are represented by following matrix

where g_m is the transconductance parameter of OTA stage and β which is ideally unity; denotes the non-ideal voltage transfer gain between ports z and w.

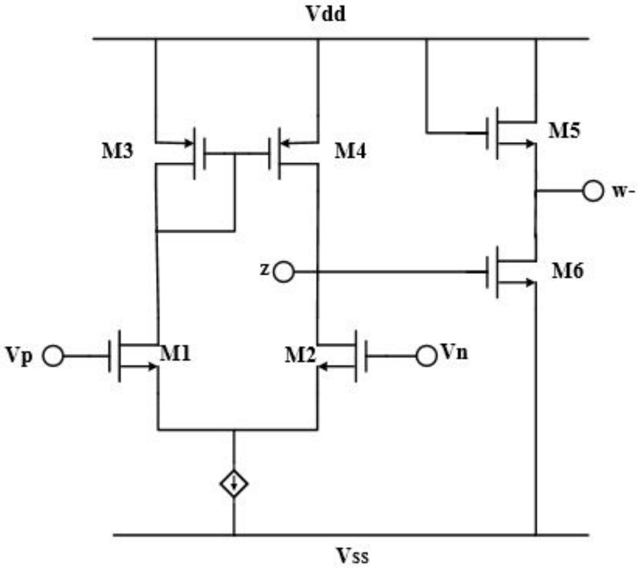

Fig.2: CMOS implementation of VDIBA

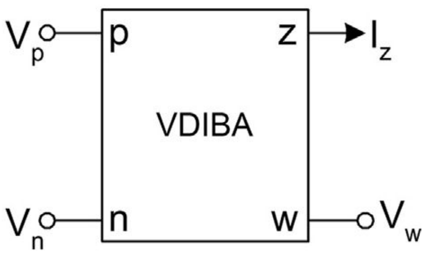

Fig.3: Symbol of VDIBA

The novel low-voltage low-power VDIBA based on LVCCCM is shown in Fig. 4. The proposed circuit uses LVCCM instead of simple current mirror to implement the OTA used in the input stage and the output stage is implemented using unity gain inverting buffer.

The proposed configuration offers many attractive features such as low static power dissipation alongwith high output resistance of the first stage .

Using analysis mentioned in [ ] the port z resistances

$$Rout = r_{o2} \,||\, r_{o41} \,||\, r_{o42}$$

Comparing equation and it can be observed that the port z resistance of the proposed structure is higher than that of the conventional structure.

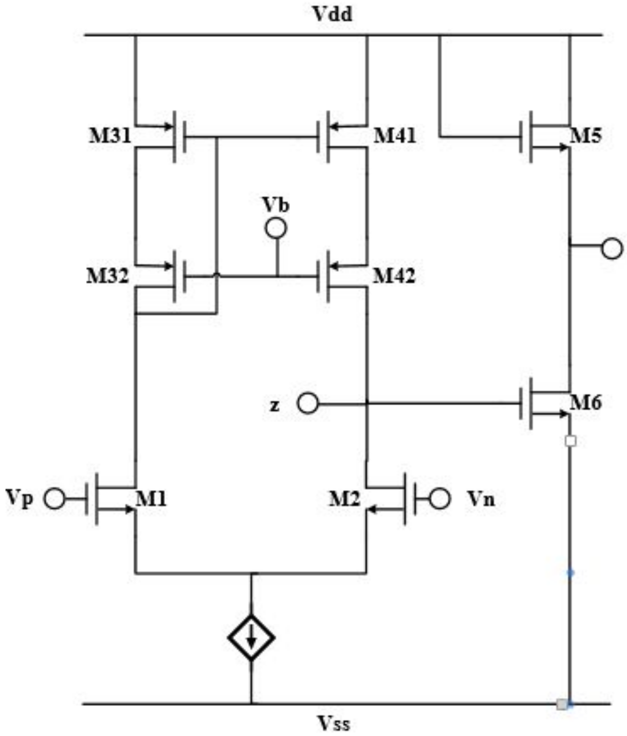

Fig.4: Proposed LVCCM based VDIBA

The transistors M31,M32,M41and M42 in the Fig.4 represents LVCCM where Vb is the biasing voltage for controlling the gates of M32 and M42.Transistors M1 and M2 are the input ports for the input supply .M5 and M6 serves as unity inverting buffered amplifier . Port z is the high impedance ouput port whereas port w is low impedance port .

IV. RESULTS AND SIMULATION

The designed circuits are simulated using CADENCE in TSMC 180nm CMOS technology using 0.7 V power supply.

The Fig.5 shows the graph between the output currentIz and input voltages Vp and Vn. The linearity can be viewed which varies from (-200mV) – (+200mV) where the biasing current is 100µA.

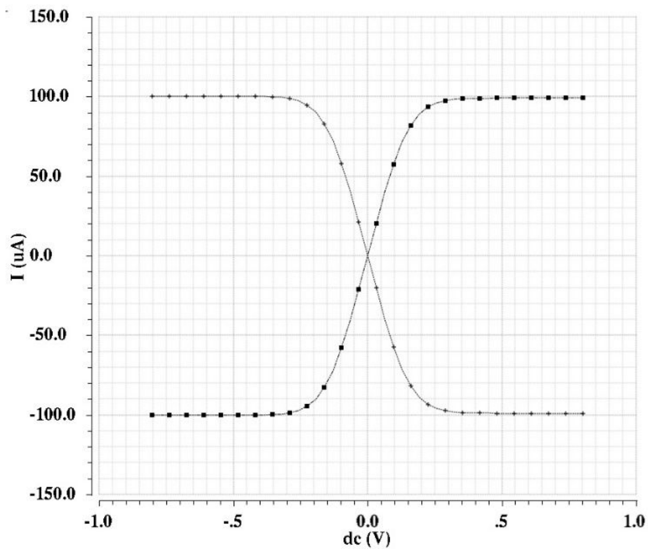

Fig.5: Linearity ofproposed LVCCMVDIBA

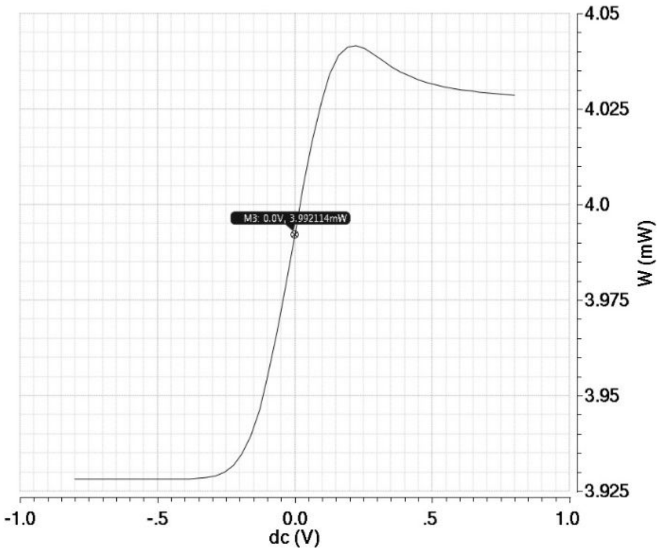

Fig.5: Power consumption ofproposed LVCCMVDIBA

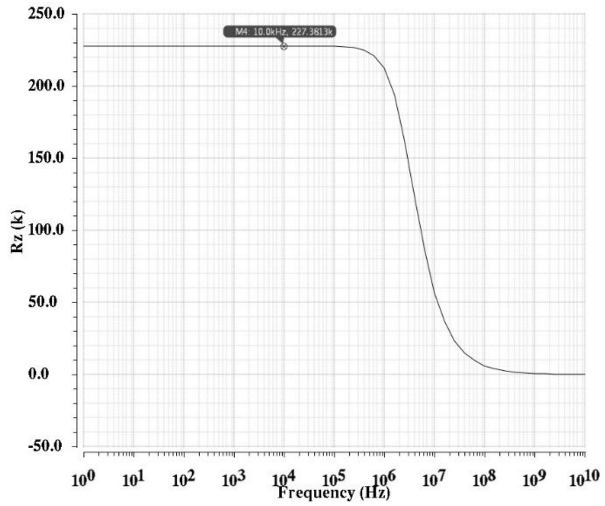

Fig.6: Output resistance Rz of VDIBA

Fig.6 depicts the output impedance at port z . The value obtained of Rz is 227 kΩ which is much better than the conventional VDIBA reported in [1].

Table 1 : Results of proposed VDIBA.

Parameters	Proposed VDIBA
Technology (mm)	0.18
Supply voltage (V)	0.7
No. of transistors	8
Linearity	(-200) - (+200)
Power consumption	3.99mW
Port z impedance (kΩ)	227

The Table.1 provides all the detailed results of simulations done on cadence of the proposed circuit .

The fig 8 tells about the power consumption of the proposed LVCCMVDIBA which is 3.99mW.

V. CONCLUSION

This paper presents LVCCM based voltage differencing inverting buffered amplifier. It operates at a lower supply voltage and has reduced power consumption. The proposed VDIBA is used in the realization of a low voltage filterapplications and several attractive features such as independently tunable filter parameters, cascadability and low sensitivity figure. Therefore, the proposed VDIBA may be useful in lowvoltage low-power analog signal processing or generation applications.

ACKNOWLEDGMENT

I would like to thank Ajay Kumar Garg Engineering College for providing all the required resources for this work and their faculty members for their guidance.

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