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IMPROVED PERFORMANCE IN CURRENT MIRROR SUITABLE FOR LOW VOLTAGE APPLICATION

Neha Singh, Richa Srivastava

***Abstract*— This paper presents a high performance current mirror (CM) in which the output current accurately copies the input current. In this paper, a low power design of current mirror using floating gate MOS transistor is presented. The proposed CM offers extremely high degree of copying accuracy over a wide operating current range. The proposed CM is being simulated by using CADANCE Virtuoso in TSMC 0.18 µm using CMOS technology, using a single supply voltage of 1.2 V. The circuit is shown to have high current copying accuracy for a range of (0–700 µA)**

***Index Terms*—.FGMOS, Compliance voltage, Low power, Current mirror.**

I. INTRODUCTION

In today's scenario, the market demands of the electronic equipment which are portable and which are efficient i.e. can be used for long period. The electronic equipment in demand consumes low power and they work on low voltage. The downscaling of the technology has been done in nanometers and demand of low power requirements under low supply voltage has put limitation on design of amplifiers with high gain, dynamic range and full signal swing [2]. In view to market demand, nowadays IC designers are moving towards Floating Gate Metal Oxide Semiconductor (FGMOS) transistor [1].

So, the main reasons for the advent of low voltage circuits can be:

(a) Firstly, to make sure about the device reliability, as the channel length is being scaled down in the sub microns and gate oxide thickness to nanometers, the supply voltage needs to be reduced. Due to the scaling of gate length which also scales down the threshold voltage and as the off state current of MOSFET varies exponentially with the threshold voltage Vt, as the Vt reduces it results in higher off state current.

(b) Secondly, increasing number of components on a single chip. Only a limited amount of power per unit area can be dissipated on a silicon chip. The increasing density of components allows more electronic function per unit area, so the power per electronic function has to be lowered in order to prevent overheating of the chip.

(c) Thirdly, battery-powered portable equipment's. In order to have an acceptable operation period from a battery, both the supply power and the supply voltage have to be reduced. The reduced power supply and the supply voltage requires the special circuit techniques.

So nowadays the challenges that are being derived from market requirements is to reduce supply and the power consumption of the circuit. Many new low voltage design techniques for low voltage analog circuits are available [5], for instance, MOSFETs operating in the:

1. Sub-threshold region [3]
2. bulk driven transistors [3]
3. self-cascode structures [3]
4. floating gate MOS (FGMOS) [2,3,13]
5. The level shifter techniques. [3]

This paper discusses characteristics of current mirror which is being based on FGMOS. This paper comprises of the following sections, in II (second) section current mirror has been described as per discussed in various literature. The FGMOS have been discussed in section III. The proposed circuit have been discussed in section IV and then in continuation with the simulation result in V.

II. CURRENT MIRROR

Current mirror is a one which is being used as a circuit for biasing purpose in operational trans-conductance amplifier (OTA), opamps current amplification, and also as active loading and level shifting [4]. A CM is a type of current amplifier which is being used to replicate the input current at its high impedance output node. It is being used widely as a basic unit in most digital and analog/mixed mode integrated circuits such as OTAs, CCIIs, OMAs, CFOAs, analog filters etc. for current amplification, biasing and active loading [6–10]. Thus, the CM helps in improving performances of the ICs. The current mirror circuit basically converts the current entering the circuit into a voltage, and then this voltage is used to control current exiting the circuit [11, 12]. In this paper, a very high performance CM operating over a wide current range has been proposed.

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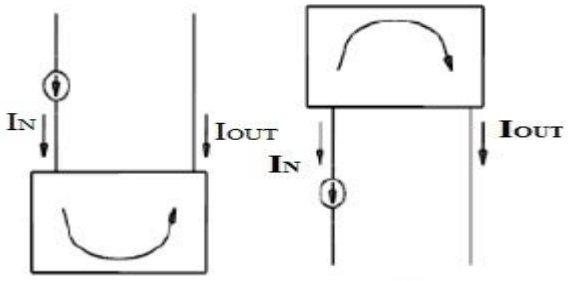


Fig 1: Block Diagram of Current Mirror.

III. FLOATING GATE MOSFET

FGMOS is floating gate metal oxide semiconductor which is being used as a low voltage design technique in analog circuits. The capacitors which are at input side in FGMOS transistors, they create a capacitor divider network which improves the linearity and attenuates the input signal. Applications in using of multi-input FGMOS transistors can be found in design of multiplier, trans conductor, filter, I–V converter, current mirror with wide range and increase in the bandwidth and other concerned characteristics required for low power design [2]. The gate of a standard MOS transistor is electrically isolated for the fabrication of a standard MOS transistor. The floating gate has a number of inputs are put or set above it, which has being isolated electrically from the floating gate. Floating gate, which is completely surrounded by resistive materials and inputs are connected to it capacitively only. So in terms of DC operating point floating gate is a floating node [13].

The structure of an N-input floating gate MOSFET is shown in figure (2). The schematic symbol is shown in figure 3(a) and its equivalent circuit is shown in fig 3(b). The input voltages are capacitively coupled to the floating gate of the MOSFET, these voltages modulate the channel current as shown in figure 3(c).

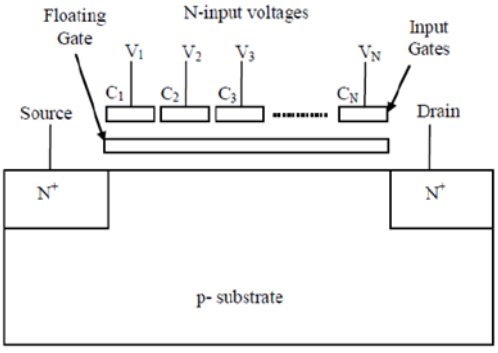
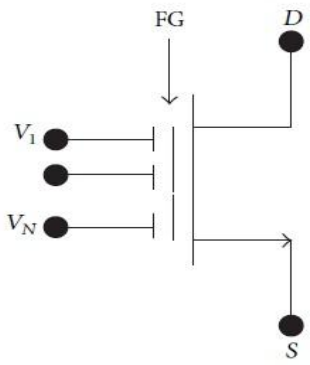
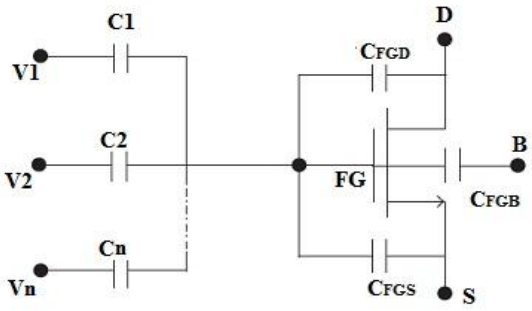


Fig 2: Structure of Floating gate MOSFET.



(a)



(b)

Fig 3:(a) schematic symbol (b) Equivalent Circuit

Now let's assume Q_{FG} is the net charge on the floating gate, V_{FG} is the voltage of the floating gate, and V_{gi} is voltage of the i_{th} control gate, thus

$$V_{FG} = (Q_{FG} + C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum_{i=1}^{n} C_{Gi}V_{Gi})/C_{TOTAL}$$

Where,

$$C_{TOTAL} = C_{FGD} + C_{FGB} + C_{FGS} + \sum_{i=1}^{n} C_{Gi}$$

IV. CADENCE SIMULATION OF FGMOS

FGMOS simulation is carried out using CADANCE virtuoso for 0.18 um technology. A two input common-source FGMOS circuit shown figure (4). The resistances are placed parallel to the capacitors and form the FGMOS.

The resistances which are R1 and R2 are selected in the range of giga ohms and capacitors C1 and C2 are selected in the range of femto farad. The value of R1 and R2 are 100 GΩ and the value of the both capacitances is 100 femto farad. There are two voltages Vb and Vg being mentioned one is bias voltage which can be varied and another is gate voltage which is kept constant. The voltage at the bias gate of FGMOS has been varied from 0 to 750 mV as shown in fig 5, enables us to vary the threshold voltage of the FGMOS and it can be observed that FGMOS can be operated at lower voltages as compared to conventional MOS. The gate voltage is being kept constant at 750mV.

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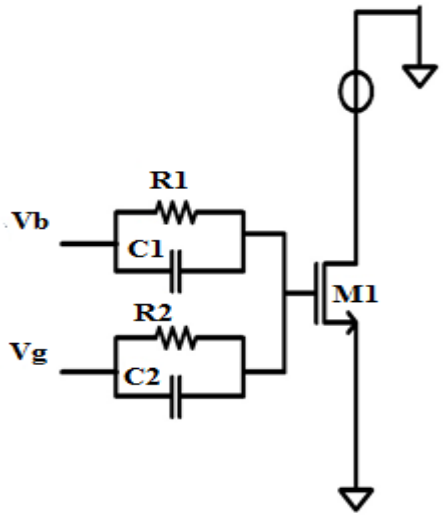

Fig 4: FGMOS circuit

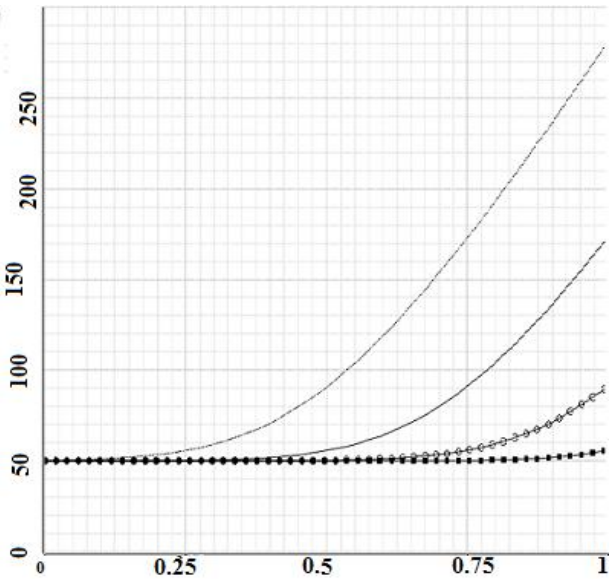

Fig 5: FGMOS Transfer Characteristics

V. PROPOSED FGMOS CURRENT MIRROR

The proposed FGMOS based current mirror configuration is shown in fig 6. The circuit consists of 6 transistor. The input current is being given through Iin of the M1 transistor and M2 is the mirror of it.

There is a FGMOS technique applied at the current mirror and it consists of two resistances, the two capacitances and a bias voltage. The circuit consists of the common source MOSFET M6 with a biasing current Ib1 as shown in fig 6. Where MOSFETS M3, M5, M6 with there biasing currents as Ib and Ib1 specifies a super cascode configuration. The table 1 defines the various design parameters of the CM which has been proposed.

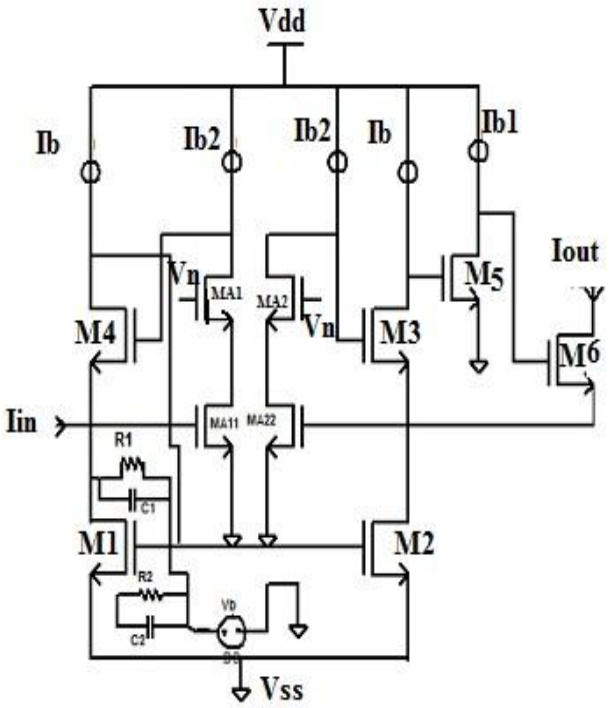

Fig 6: Proposed Current Mirror

Table 1: Design parameters of the proposed CM

VI. SIMULATION RESULTS

In this section, simulation results of the proposed CM have been presented. The proposed circuit has been simulated by Cadence Virtuoso in TSMC 0.18 lm CMOS technology, using a single supply voltage of 1.2 V.

The fig7 shows the graph between the output current and input current. The current transfer characteristics of proposed circuit from 0to700 µA is shown in Fig. 7 It shows the input current ranging from 0 to 700uA as compared to conventional which has range from 0 to 500uA.

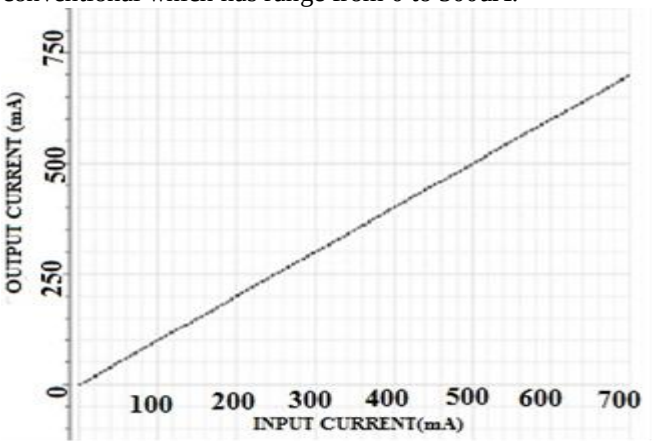

Fig 7: Input current vs Output current characteristics of proposed current mirror

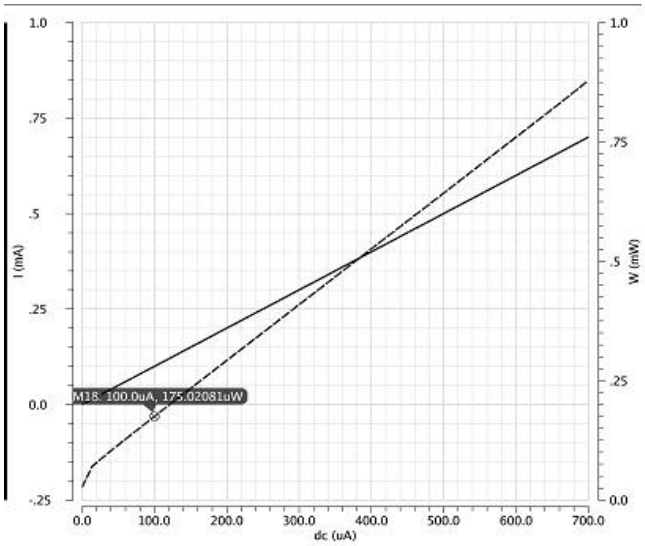

Fig 8: Power consumption of the proposed CM

The fig 8 tells about the power consumption of the proposed CM which is 175uW.

Table 2: Simulated results for proposed CM

Parameters	Proposed CM
Technology	0.18um
Power supply	1.2V
Input current range	(0 – 700)uA
Power consumption	175.02uW

VII. Conclusion

This paper demonstrates a current mirror (CM) employing FGMOS technique. The FGMOS technique helps in improving the current range at low voltages and improves power consumption of the CM. The CM can be used in current amplification, biasing and active loading.

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