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A LOW POWER CMOS 3-BIT FLASH ANALOG TO DIGITAL CONVERTOR USING 90NM TECHNOLOGY

Mary Kamala Vegesina[1], Bala Krishna Konda[2]

[1]M.Tech (DECS), Department of Electronics & Communication Engineering, Eluru College of Engineering & Technology, Eluru, AP, India

[2]Assistant Professor, Department of Electronics & Communication Engineering, Eluru College of Engineering & Technology, Eluru, AP, India

Abstract— ***High-speed, low-to mid-resolution analog-to-digital converters (ADCs) are required for many applications, such as high speed wireless and wireline communications, digital oscilloscopes, and radar.***

The flash ADC architecture is commonly used to implement ADCs for such applications. Flash ADCs consist of a large bank of comparators operating in parallel and each comparator must meet a strict input offset specification. To meet the input-offset specification with Minimal power and are an overhead, comparator calibration techniques are required. Double-Tail Latch Type comparator is drawback the clk and clkb requires high accuracy timing because the latch stage has to regenerate the differential input voltage coming from Input stage at very limited time. The Proposed Comparator using ADC circuit is more compact than the previous design. Power, processing time, and area are all minimized. This design can be used for modem high speed ADC applications.

Keywords:-CMOS comparator, CMOS Analog Integrated Circuit, Flash Converter, priority encoder.

I. INTRODUCTION

With the advancement of technology, digital Signal processing has progressed dramatically in recent years. Signal processing in digital domain provides high level of accuracy, low power consumption and small silicon area besides providing Flexibility in design and programmability. The design process is also quite faster and cost effective. Furthermore, their implementation makes them suitable for integration with complex digital signal processing Blocks in a compatible low-cost technology, particularly CMOS. This evolution of technology Provides much faster transistors with smaller sizes, making it possible to have very high clock rate in digital circuits. In the end, it leads us to design a very high speed as well as systems with small die area called system oa

chip (SoC), with a smaller number of chips using increased integration level. However, the evolution of technology has Not provided same level of benefit for the analog circuit design. So to extract the advantages of digital signal processing, there is a trend of shifting signal processing from Analog to more efficient digital Domain and dealing with the analog signals only in the input-output stages. This has resulted in the requirement of smart converters between analog and digital signals to cope up with the evolution of technology.

Recent in many wireless mobile applications demand very high speed data converters with wide bandwidth, higher signal to noise ratio and variable (adaptive) resolution with optimized power and cost effectiveness. So there is a need for upgrading the performance of data converters to meet the demands of Emerging technologies. So it is a challenging issue in the mixed signal design to have high speed, variable resolution Data converters with less space and low power consumption. There are many challenges for ADCs to be adaptable for SoC implementation with current mixed-signal technology.

The major considerations in designing ADCs for the complete So Care high speed, low voltage, and low power consumption. In the portable device market, reducing the power consumption is one of the main issues. ADCs should be integrated with digital circuits on a single chip for the portable devices. All battery Powered devices are now being designed to include low power techniques to prolong the battery life. Similarly, ADCs need low power architecture or a low power technique. Low voltage operation is one of the difficult challenges in the mixed-signal ICs. The down-scaling of the minimum channel length to 0.065um

results in the reduction of the Analog power supply voltage to2.5V.However, the minimum supply voltage for the analog circuits predicted in SIAR oad map [1] [2] does not follow the digital supply voltage reduction. A mixed-signal circuit designer faces a great challenge when designing an ADC that operates at low voltage because of the relatively high threshold voltage of the transistors. As a result, an ADC should be operated in a small voltage range. The main focus of this is on designing an ADC that is truly variable-resolution and variable-power. It should operate at higher speed under low resolution while also consuming less power. Such features are highly desirable in applications such as wireless and mobile communications.

2. CONVENTIONALCOMPARATOR

2.1 Dynamic comparator

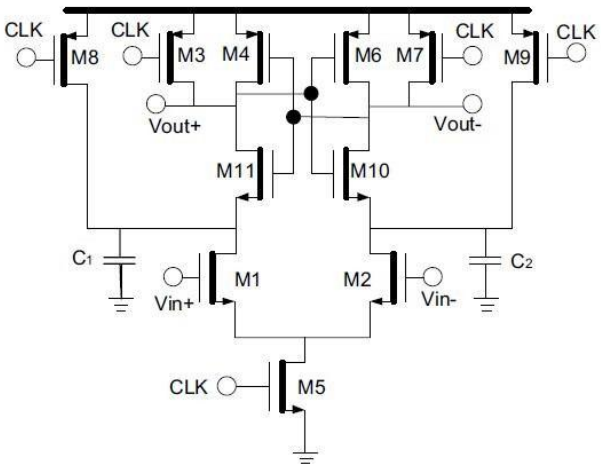

Figure 2.1: Dynamic Comparator

2.2. Double-Tail Latch Type comparator

Figure2.2 shows the schematic of the Double-Tail Latch type Voltage SA. Double-Tail derived from the fact that the comparator Uses one tail for input stage and another for latching stage. It has less tacking and can therefore operate at lower supply voltages [3].Large size of the Transistor M12 enables large current at latching stage which is independent of Common mode voltages at inputs and small size of M1 offers lower supply voltages resulting lower offset

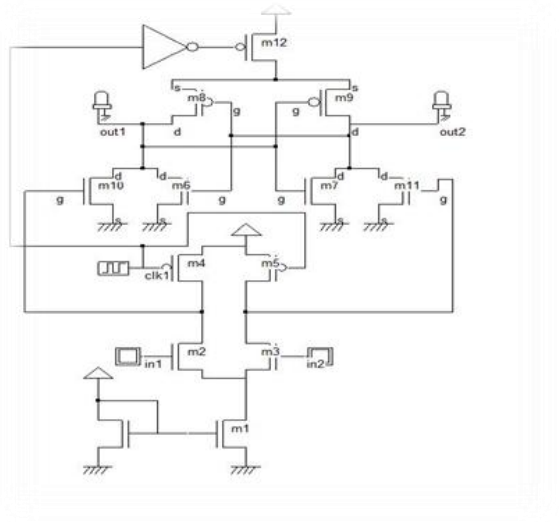

Figure 2.2. Double-TailDynamiccomparator

During rest phase (clk=0V), M4 and M5 charges to VDD which in turn charges Ni nodes to VDD. Hence M10 and M11turn On and discharges output nodes to GND. During evaluation phase (clk=VDD), the tail current transistors M1

And M12 Turns ON. On Ni nodes common mode voltage decreases and one input dependent differential mode Voltage generates. M10 and M11 pass this differential mode voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Di nodes is no longer high enough for M10 and M11 to clamp the outputs to ground [3].M10 and M11 also provide additional shielding between the input and output which in turn reduces kickback noise. Double-Tail Latch Type comparator is drawback the clk and Clkb requires high accuracy timing because the latch stage has to regenerate the differential input voltage coming from Input stage at very limited time. Now if we replace the clkb with the inverter whose input is clk signal then Clk has to drive heavier load in order to drive largest transistor M12 in a smallest possible delay. Now if clkb leads clk, then comparator will undergo increased power dissipation and if clkb lags clk, it results in increased delay means less speed of operation due to short circuit current path from M12 to M10/M11 through M8/M9.

3. PROPOSED COMPARATOR: ENERGY EFFICIENT TWO STAGE COMPARATOR

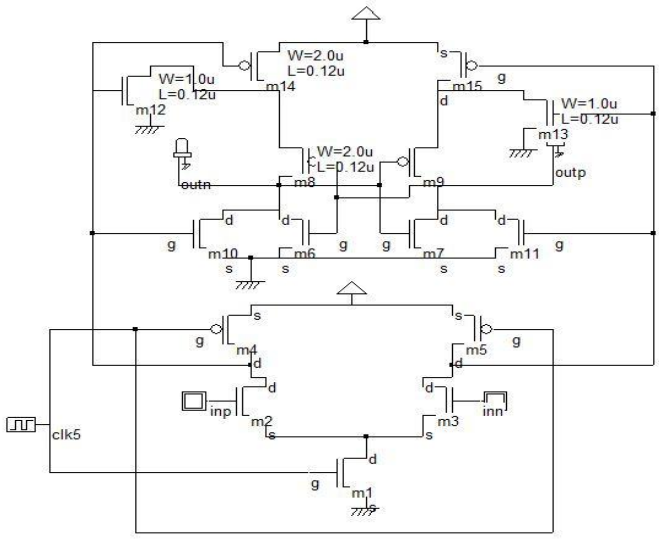

Figure 3.1: Proposed Comparator\

Figure3.1 shows the energy efficient two-stage comparator. The circuit is almost same as Figure.2.2 except the output latch stage. By modifying the output latch stage during reset phase(clk=0V and clkb=VDD),the drain diffusion capacitances of PMOS transistors M14 and M15 & NMOS transistors M2 and M3 is much lesser than the Ni node capacitances. And hence it can be operated in lesser power dissipation and higher speed than the previous comparator. But still the clocking problem was not solved since clk and clkb is operating in same clock signal as that was in previous comparator.

4. RESULTS AND DISCUSSIONS

To compare the performance of the proposed comparators with previous works, each circuit was simulated in DSCH &Micro wind Tool. Technology Used in CMOS Simulation outputs 90nm technology with VDD=1V as supply voltage. The layout diagrams show the result summary after post layout simulation. From table1 is ADC design Compare previous comparators &proposed comparator is verified the Power & delay.

Table 1.Compare the Different Types ADC

Parameter	No.of Transistor	Power(mW)	Delay(Ps)
ADC using Dynamic Comparator	267	1.414	300
ADC using Double-Trail Comparator	295	2.053	141
ADC using Proposed Comparator	295	1.057	134

Table 2.Compare the Different Types comparators

Parameter	No. of Transistor	Power(µW)	Delay(Ps)
Dynamic Comparator	11	7.23	82
Double-Trail Comparator	15	0.694(m W)	76
Proposed Comparator	15	10.7	67

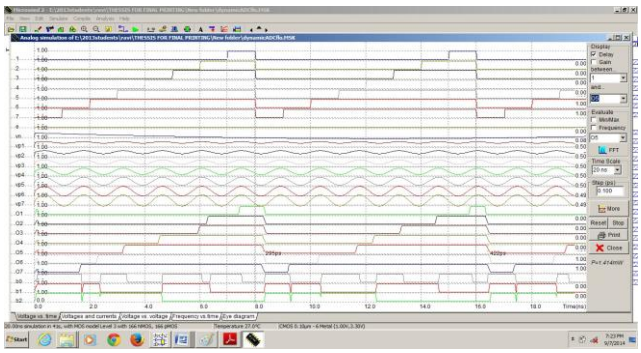

Figure 4.1: Simulation Results of ADC using Dynamic comparator

Figure 4.2: Simulation Results in ADC using Double-Tail Dynamic comparator

Figure 4.5: Simulation Results in ADC using Proposed Comparator

5. CONCLUSION

A3-bit Flash ADC Using Proposed Comparator. The Accuracy of this Flash ADC is enhanced by a digital Calibration scheme this paper has demonstrated the effectiveness of the calibration scheme. Proposed ADC design is low power, high permanence compare to conventional ADC.

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First Author:- Vegesina Mary Kamala M tech (DECS) final year, Department of Electronics and Communication Engineering, Eluru College of Engineering and Technology, Eluru Andhra Pradesh, INDIA

Second Author:- Bala Krishna Konda Assistant Professor, Department of Electronics and Communication Engineering, Eluru College of Engineering and Technology, Eluru Andhra Pradesh, INDIA