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Design and Comparison of 4 bit Arithmetic Logical Unit Using different Decoding Technique

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***Abstract*— With the scaling of technology and the need for high performance and more functionality, hardware constraints becomes a major bottleneck for microprocessor systems design. In this paper, comparison on the basis of hardware consumed, time taken has been made between ALUs having different coding techniques. Firstly, in an ALU's decoder one hot decoding technique is implemented, which is very efficient for time saving. Secondly, the decoder having gray coding technique is executed this technique has very high impact on the amount of reduction of hardware constraints and the amount of time consumption. Lastly, binary coding is used in decoder and the result is observed. Functionality of proposed ALU implemented on FPGA is tested using Xilinx tool. Analysis of the consumption of hardwiring has been checked by using rtl schematic diagram of Xilinx.**

***Index Terms*— LUTs(look up tables), slice registers, IOBS(input output buffers) , FPGA, RTL**

I. INTRODUCTION

Designing of an alu can be done in multiple ways .Designing is done by the user according to the usage and implementation of the alu. But the hardware usage and amount of time taken for implementation always has a higher priority for every designer. In this paper we are comparing the number of luts, iobs, slice registers and time taken by different codes.

Designing an alu is the most common and challenging task for every digital logic designer. One of the key factors for optimizing an alu design is the choice of state coding, which influences the complexity of the logic functions, the hardware costs of the circuits, timing issues, power usage, and many more. There are several options like binary encoding, gray encoding, one-hot encoding. The choice of the designer depends on the factors like technology, design specifications, etc.

The variation in final outcome is number of iobs, luts and time consumption is determined by coding a 4 bit alu. In this experimental setup different codes are coded in verilog Xilinx for the working of 4 bit alu. To meet design requirements (such as speed, area, and power requirements), one may need to modify the original HDL sources or change synthesis and implementation options.

Performing such changes sometimes requires understanding the impact of these changes in the final implementation. The Schematic Viewer can help in these situations, because it allows visualizing and comparing different design net lists. So the final comparison is made on the basis of rtl schematic viewer.

II. EXPERIMENTAL SETUP:

The four bit alu consists of one rom having predefined values for alu input, one decoder for selecting the function to be formed by alu and one logical unit having 16 operational functions.

FIGURE 1 BLOCK DIAGRAM OF AN ALU

As shown in figure 1 the rom has some predefined values that has to be sent to alu and decoder.rom is of 12 bits out of which first 8 bits goes to alu and last four bits to decoder. Decoder takes the 4 bits and selects the function to be performed by an alu by decoding techniques. Alu when receives the values from rom and from decoder it performs the selected function and gives the desired outcome.

As visible the decoder can be coded in different ways depending on the usage and need. The three different ways are shown and compared in this paper.

III. VARIOUS CODING TECHNOLOGIES:

A. *One hot coding technique:*

In one hot encoding only one bit of the state vector is asserted for any given state. All other state bits are zero. Thus if there are n states then n state flip-flops are required. As only one bit remains logic high and rest are logic low, it is called as One-hotencoding.

Example: If there is a FSM, which has 5 states. Then 5 flip-flops are required to implement the FSM using one-hot encoding. The states will have the following values:
S0 -10000
S1 -01000
S2 -00100
S3 -00010
S4 -00001

Advantages of one hot coding:

- State decoding is simplified, since the state bits themselves can be used directly to check whether an alu is in a particular state or not. Hence additional logic is not required for decoding, this is extremely advantageous when implementing a big alu.
- Low switching activity, hence resulting low power consumption, and less prone to glitches.
- Modifying a design is easier. Adding or deleting a state and changing state transition equations can be done without affecting the rest of the design.
- Faster than other encoding techniques. Speed is independent of number of states, and depends only on the number of transitions into a particular state.
- Finding the critical path of the design is easier (static timing analysis).
- One-hot encoding is particularly advantageous for FPGA implementations. If a big design is implemented using FPGA, regular encoding like binary, gray, etc will use fewer flops for the state vector than one-hot encoding, but additional logic blocks will be required to encode and decode the state.

Disadvantages of one hot coding:

- The only disadvantage of using one-hot encoding is that it required more flip-flops than the other techniques like binary, gray, etc. The number of flip-flops required grows linearly with number of states. Example: If there is a FSM with 38 states. One-hot encoding requires 38 flip-flops where as other require 6 flip-flops only.

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B. *Gray coding technique:*

The reflected binary code, also known as Gray code after Frank Gray, is a binary numerical system where two successive values differ in only one bit. The reflected binary code was originally designed to prevent spurious output from electromechanical switches. Today, Gray codes are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems. Thus the power dissipation due to charging and discharging of the clock at unused gates, is avoided in this strategy.

Take an example where say n bit data is coming from block A running at 100 Mhz, and going to a block B running at 1333Mhz.So to send the data from one clock domain to the other, people use fifo. Now to reliably tell how much data is in the fifo which is being clocked by A clock i.e 100 MHz, the write pointer of the fifo would have to be read by a block B running at 133Mhz. So I will use gray coded counters for this fifo pointer instead of normal binary coded counters, so that block B running at 133MHz could reliably capture the value of this pointer, which is being clocked at 100Mhz. Since only one bit is going to change, for every count change are very reliable.

These will use the same number of FFs as Binary Encoding, but it has a great advantage over binary in cetrain cases. Because it has a hamming distance of 1 between two codes, it is a very reliable count. i.e only one bit changes when the count advances. So it is used in Address counters for fifos, when implementing an interface between 2 Async Clock domains.

C. *Binary coding technique:*

A binary-coded decimal system provides rapid binary-decimal conversion. However, BCD arithmetic operations are often slow and require complex hardware.

In computing and electronic systems, binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digits represented by a fixed number of bits, usually four or eight, although other sizes (such as six bits) have been used historically. Special bit patterns are sometimes used for a sign or for other indications (e.g., error or overflow).
There are different weighted codes in binary system like 8421, 2421, 5211 . the codes for the system vary according to the weighted codes used. The weighted codes used for this binary coding technique is 8421 weighted codes.

The code of a state is simply a binary number. The number of bits is equal to log2(N) rounded to next natural number. Suppose N = 6, then the number of bits are 3, and the state codesare:

S0 - 000
S1 - 001
S2 - 010
S3 - 011
S4 – 100

IV. SYNTHESIS RESULT:

The best known and most believable method of determining the answers to the questions posed in the introduction is to experimentally synthesize real circuits using a CAD flow into the different FPGA architectures of interest, and then measure the resulting area and time consumed. This rtl view is register transfer level view. From this view we can get the clear idea about final implementation of the codes on the processor chip. The user can determine the need of his processor on the basis of the conclusion obtained from the table.

Table 1: Device utilization

Device utilization			
Logic utilization	**One hot coding technique**	**Gray coding technique**	**Binary coding technique**
Number of slice registers	9	1	1
Number of slice luts	113	13	10
Number of fully used lut-ff pairs	9	1	1
Number of bonded IOBS	12	11	11

- The amount of change on final implementation is clearly visible. The number of luts and slice registers have been decreased drastically.
- The number of slice registers also decreases from 9 registers to 1.
- Compared to number of luts in one hot coding i.e 113 the number of luts in gray coding hase been reduced to 13. One more lut gets reduced when binary codes are implemented.
- Number of fully used luts –ff pairs also decreases from 9 to 1.
- This comparison shows that the different system of coding can have a very massive impact on the final outcome.

V. RTL SCHEMATIC VIEW:

A. One hot coding technique

As shown in figure 2 this is the rtl hardware schematic diagram of one hot coding. As seen from the figure number of luts required is very large. The number of data lines used is also many. If this is implemented on the chip then the area consumption will increase in large number. Which is the basic drawback.

One Major advantage for using this technique is time consumption. On implementation of testbench for one hot

coding technique the time consumed for getting final output was lesser then binary and gray coding techique.

As the number of mux required by the one hot coding technique is different for every bit the time consumption reduces. But the amount of hardware increases.

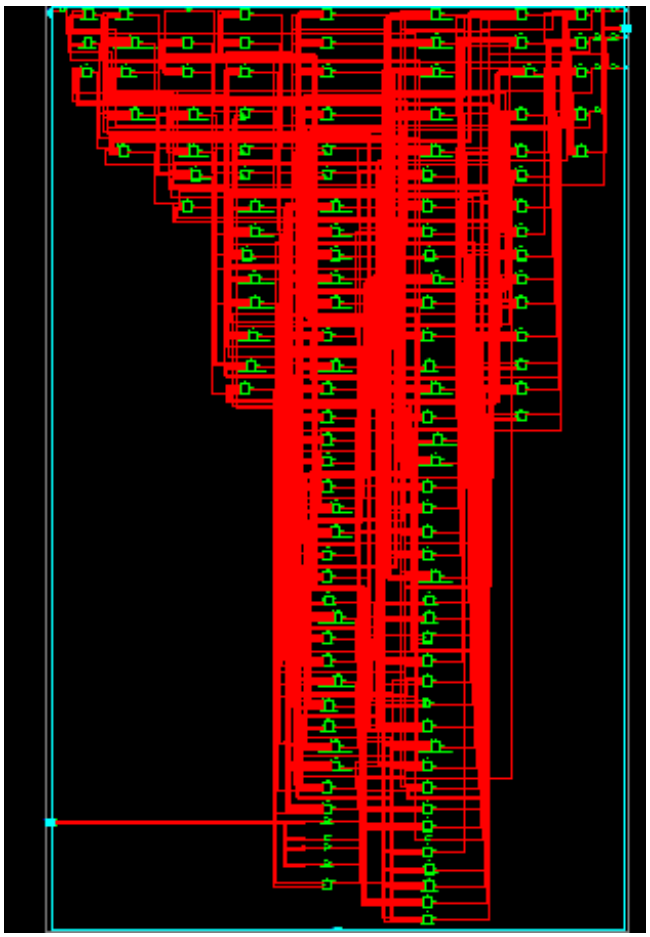

Figure2. : RTL schematic view of One hot coding technique:

B. Gray coding technique:

As cited in figure 3 Gray coding rtl technological schematic view it has very small hardware usage. It has only 13 luts for its functioning. This is a major criteria for selcting the coding technique.

On implementation of testbench for gray coding technique the amount of time taken is more than one hot coding.

Because the implementation of the codes where only on 4 bit alu so major difference intime consumption wsa not visible. Had it beean a bigger alu for example 32 bit then time constraint would have been a big issue.

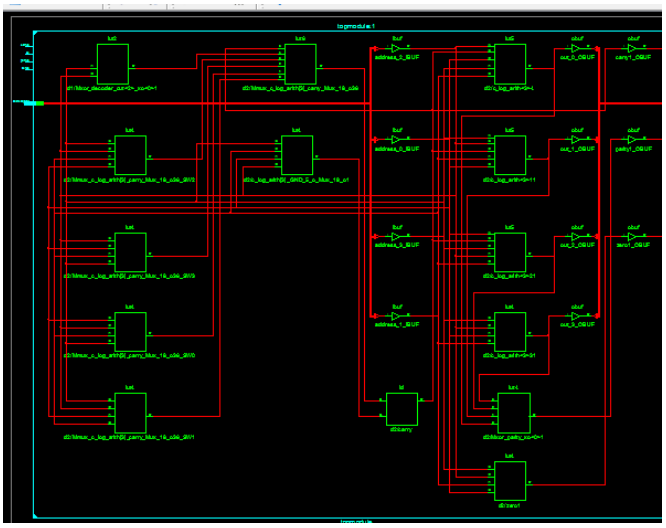

Figure 3: RTL schematic view of gray coding technique

C . Binary coding technique:

Figure 4 shows the schematic view of binary coding technique. In this technique the number of luts consumed is lowest and the time consumed by binary and gray coding is same. But the time consumed by binary coding is more than the one hot coding method.

In binary technique the logic is very simple so it does not need any technical person to understand the system. The codes requires only one mux for implementation so all the lines first goes to that mux and then the selected line gets implemented. So the time consumed is higher.

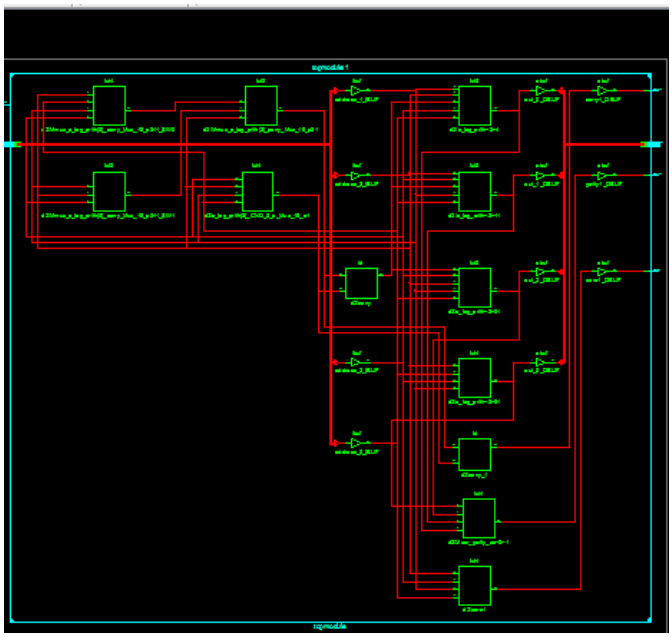

Figure 4: RTL schematic view of binary coding technique

VI. CONCLUSION

From this paper, we can say that the choice of coding technique applied has immense effect on the final outcome. The rtl schematic shows the final output from which the result is clearly visible. The number of luts changes drastically and thus the amount of hardware consumed can be decreased. As the number of luts decreases the amount of slice registers and fully used lut- FF pairs also decreases. Moreover, the time consumed by the alu to derive the result varies. It is smaller in hot coding technique then in gray and binary coding technique.

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REFERENCES

Samir palnitkar "Verilog hdl a guide to digital design and synthesis"
[1] T.R. padmanabhan and B. Bala Tripura sundari "Design through Verilog Hdl"
[2] Stephen D brown " Fundamentals of digital logic with Verilog"
[3] http://www.asic-world.com/verilog
[5] Jason H. Anderson and Farid N. Najm "Power-Aware Technology Mapping for LUT-Based FPGAs"
[6] Elias Ahmed and Jonathan Rose "The Effect of LUT and Cluster Sizeon Deep-Submicron FPGA Performance and Density".
[7] A Comparative Study", In Process. of the IEEE Student Conference on Electrical, Electronics and Computer Sciences 2012, 1-2 Mar 2012, NIT Bhopal, India.
[8] Toshio Fujisawa, et al, "A Single-Chip 802.11a MAC/PHY With a 32-b RISC Processor", in IEEE Journal Of Solid-State Circuits, Vol. 38, No. 11, November 2003.
[9] J. R. Allen, et al, "IBM PowerNP network processor: Hardware, software, and applications," in IBM Journal of Research & Development, Vol. 47, No. 2/3 March/May 2003.
[10] Xiaoning Nie, et al, "A New Network Processor Architecture for High-speed Communications," in IEEE Workshop on Signal Processing Systems, 1999.

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