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Single Ended Read Disturb-Free and Differential Write based Low Power SRAM cell with Enhanced Noise Margin

Arjun S. Yadav*, Sangeeta Nakhate

***Abstract*—The SRAM cell static noise margin is a major problem of nano-regime MOS technology due to scaling of supply voltage. This paper analyses the performance of novel PPN inverter based 8T SRAM cell. In which the read driver is a part of latch that supports read disturb-free operation during read and PPN stacking effect offers reduction in leakage power and enhancement in noise margin. The simulation results include analysis of design parameters such as read static noise margin, write static noise margin, read delay, write delay, leakage power dissipation and layout area. The proposed cell offers 16% (5%) improvement in write static noise margin as compared with existing 6T (SE9T) as well as offers 7% smaller leakage power consumption compared to 6T, 8T and ER9T. For fair comparison, we have considered array of 256×32 cell for justification.**

***Index Terms*— read disturb-free, read static noise margin, leakage power dissipation, write static noise margin.**

I. INTRODUCTION

SRAM cells array occupy 90% of total chip area and dominate the leakage power consumption. The repetitive downscaling of the process technology by 0.7× has improved the integration density up to twice of its actual value [1]; however, this downscaling cause severe leakage power dissipation. The most popular battery-powered portable devices such as medical instruments, wireless module sensing networks and smart phones requires small size power unit because of light weight constraints. To overcome this problem, pull-down the supply voltage is the most effective technique to reduce energy consumption because dynamic power consumption proportional to square of VDD and static power proportional to VDD. The device scaling along with the supply voltage scaling improve the power performance of SRAM but serious problems such as read static noise margin (RSNM) and write static noise margin (WSNM) degrades the performance. Therefore, the SRAM cells with the enhanced static noise margin (SNM) become a first selection criterion in low-operating voltage platform.

The conventional six transistor SRAM cell not able to perform read disturb free operation because of bitline discharge through the transistor of storage latch that may boost-up the voltage of storage node which store '0' produced by the voltage division between the access devices and the pull-up devices. Furthermore, the appropriate size ratio of the access devices and the pull-up devices strictly required to obtain moderate RSNM and certainty of successful write operation. For improving the RSNM and WSNM of conventional 6T, independent read access mechanism is employed in many SRAM cells [2]. But independent read mechanism improves RSNM but performance parameters such as static leakage power consumption and WSNM of SRAM cell still poor. To overcome this issue, in the proposed design stacking of PPN transistor is used for one inverter design in storage latch. This PPN stacking offers less leakage and wider write static noise margin without disturbing important parameters like read static noise margin and layout area compared to existing cell[3-5].

The remainder part of this paper is organized in following sequence. The existing and proposed 8T SRAM cells are explained in Section 2. In Section 3, the simulation results and its comparisons are elaborated. In the last, the outcomes of paper are discussed in conclusion section.

II. EXISTING AND PROPOSED 8T SRAM CELL

The proposed single ended (SE) read disturb-free and differential write based 8T SRAM bit cell, and compared with its differential counterpart standard 6T SRAM cell and other existing SE read SRAM cell.

Fig.1(a) shows the schematic of a differential read and write based conventional six transistor SRAM cell (hereafter called 6T) [2]. In which two back to back connected inverter pair is used to provide positive feedback loop to hold the bit. Here two access transistor pair is used to allow read and write operations. This cell offers considerable RSNM and WSNM for bulk technology but with scaled technology less than 100nm, conventinal 6T cell doesn't offers conderable SNM. This cell suffer with the severe leakage due to upsized MOS are used to maintain considerable RSNM and WSNM.

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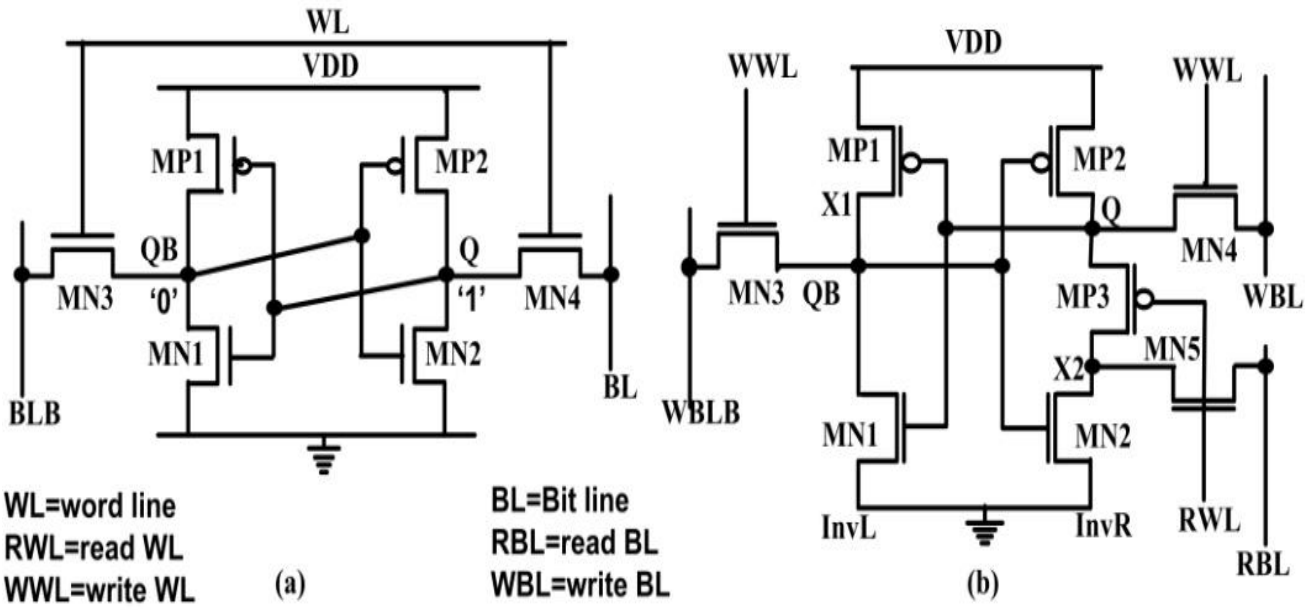


Fig. 1 Schematic of (a) 6T [2], (b) Proposed 8T

In order to provide the sufficient RSNM in the sub-nanometer technology, the read disturb free 8T SRAM cell (hereafter called 8T) has been proposed in [3]. this cell uses a additional read buffer to make read and write operations independent. The 8T cell have separate single ended read bitline (RBL) for read. Here, size of pull-down and access transistor does not affect the RSNM but still there is a problem of higher leakage and smaller WSNM remains same.

To overcome leakag issue, single ended subthreshold 9T SRAM cell (hereafter called SE9T) is proposed in [4]. In this cell extra stack transistor is placed between storage latch pull-down transistor and GND. The subthrehold SRAM cell offers ultra-low power consumption. Unfortunately, this cell also suffer from a severe increase in access latency and more vulnurable to process and temperature variations. Therefore, this is not a right choice for low power design.

In order to improve read delay with high RSNM value such as in [3-4], novel enhanced read 9T SRAM cell (hereafter called ER9T) is proposed in [5]. This cell reduces the stacking of transistor in RBL discharge path. This feature reduces the read delay upto half as provided by 6T[2] and 8T[3]. This design needs extra control circuitry to produce control signal RWLA and RWLB at expense of enahced layout area and complexity.

As discussed in the related work, existing cell[2-5] are not able to offers high SNM, and low leakage power consumption in single design. In the proposed design, the WSNM and leakage power consumption of the celll also improved without increase in layout area as compared with 8T[3] and ER9T[5].

The proposed 8T SRAM cell is based on 8T[3] SRAM cell as dipicted in Fig.1(b). compared to 8T SRAM cell stricture, we have merged storage latch and read driver using stack transistor MP3. This stack transistor will be ON during idle/write mode offers smaller leakage and higher WSNM while OFF during read mode offers indeperndent read without disturbing latch. Table 1 shows the status of all the control signal during various modes such as read, write and idle mode.

Table 1. True table of proposed 8T cell

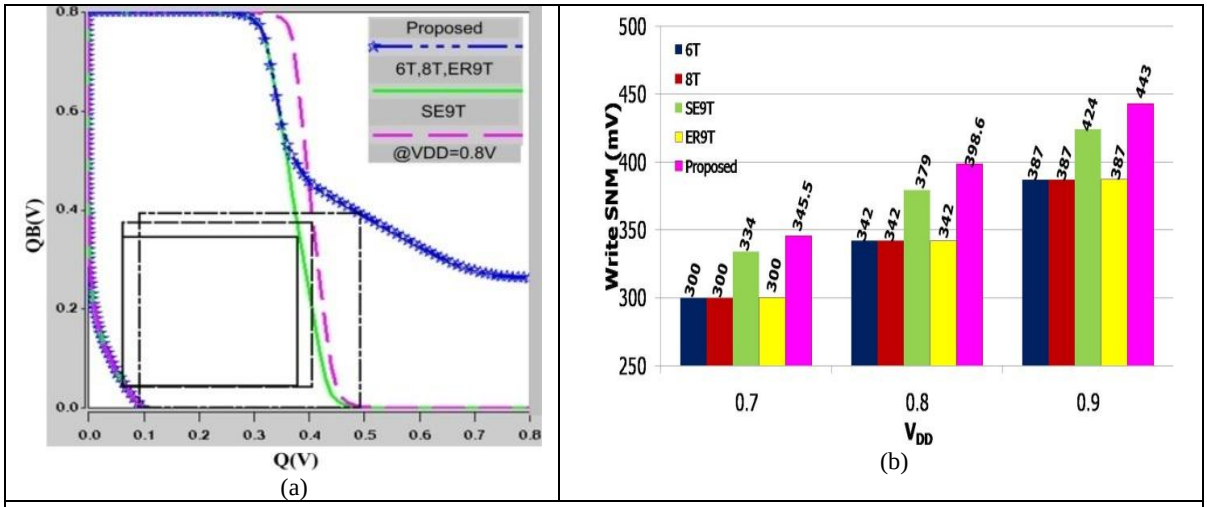
	READ	*WRITE-0*	*WRITE-1*	*HOLD*
WWL/WBL	0/0	1/0	1/1	0/0
RWL/RBL	1/1	0/1	0/1	0/1

III. SIMULATION RESULTS AND ITS COMPARISONS

The complete simulation performs on HSPICE by using 22nm MOS technology as provided by predictive technology model [6, 7]. For better comparison, varies the supply voltage from 0.7V to 0.9V.

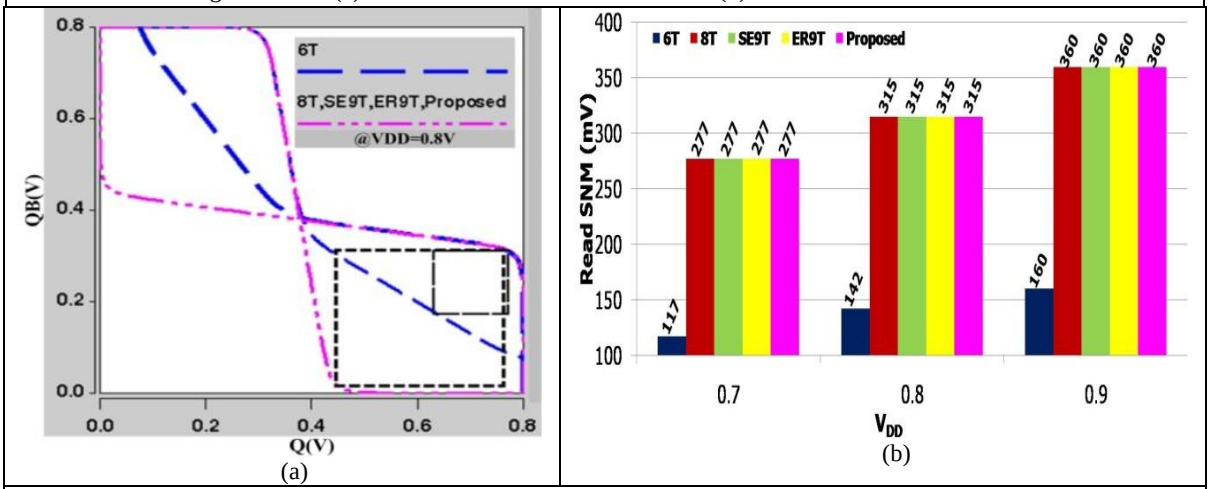
A. Write Static Noise Margin (WSNM)

The WSNM is defined as the maximum noise voltage needed to flip the cell state [8]. The proposed cell offers two values of WSNM because of the asymmetrical structure of the storage latch. The write '1'(at WBL) margin of the proposed SRAM cell is equal to VDD while write '0' margin is less than VDD. Among two values of noise margin smallest value is called as proposed cell WSNM. Existing cell obtain similar WSNM in case of write '0' and write '1' with the lowest WSNM because of the access transistor and positive feedback loop form by inverter pair. The proposed 8T SRAM cell gains 5% and 16% higher WSNM compared with 6T And SE9T Respectively at VDD = 0.8V (as shown in Fig. 2).



(a) (b)

Fig. 2 WSNM (a) charateridtics curves at VDD=0.8V (b) measurment at different VDD



(a) (b)

Fig. 3 RSNM (a) charateridtics curves at VDD=0.8V (b) measurment at different VDD

A. *Read Static Noise Margin (RSNM)*

In the conventional 6T SRAM cell, stored state at node (Q/QB) in the latch may flip if the voltage at node storing'0' higher than the input switching threshold of other inverter [9]. To overcome this problem, independent read driver based SRAM cells have provided in the exiting literature. The proposed SRAM cell offers similar RSNM as 8T and ER9T (as shown in Fig.3).

B. *Write and Read Delay*

In the proposed design, there is no active feedback loop exist in the storage latch during read. Similarly, write '1' offers shorter write time than write '0'. Since there is no fully active positive feedback loop exist. The proposed cell offers similar write delay (during write'0') as compared to 6T, 8T, SE9T and ER9T SRAM cell (as shown in Fig.4(a)).

The entire SRAM cell considered for comparison based on SE read. The proposed SRAM cell offers 20% penalty in read delay due to 1.2× increase in BL/BLB capacitance as compared to 6T, 8T and SE9T SRAM cell (as shown in Fig.5(b)).

C. *Leakage power*

In SRAM array, most of the cells are not accessed regularly. Most of the cells hold the state of cell until next write will not perform. This hold state power dissipation takes place due to leakage current. Therefore, the total power dissipation can be minimized by lowering the leakage power consumption of hold state. The comparison of static power dissipation is shown in Fig. 5. The proposed reduce the leakage power dissipation by 7% due to stack of P-P-N transistor configuration form at one of the inverter used for storage latch design.

D. *Layout Area*

The layout of the proposed cell is not shown in the paper due to lack of space. The proposed cell occupies similar area as existing 8T, SE9T and ER9T while occupy 30% higher layout area than 6T.

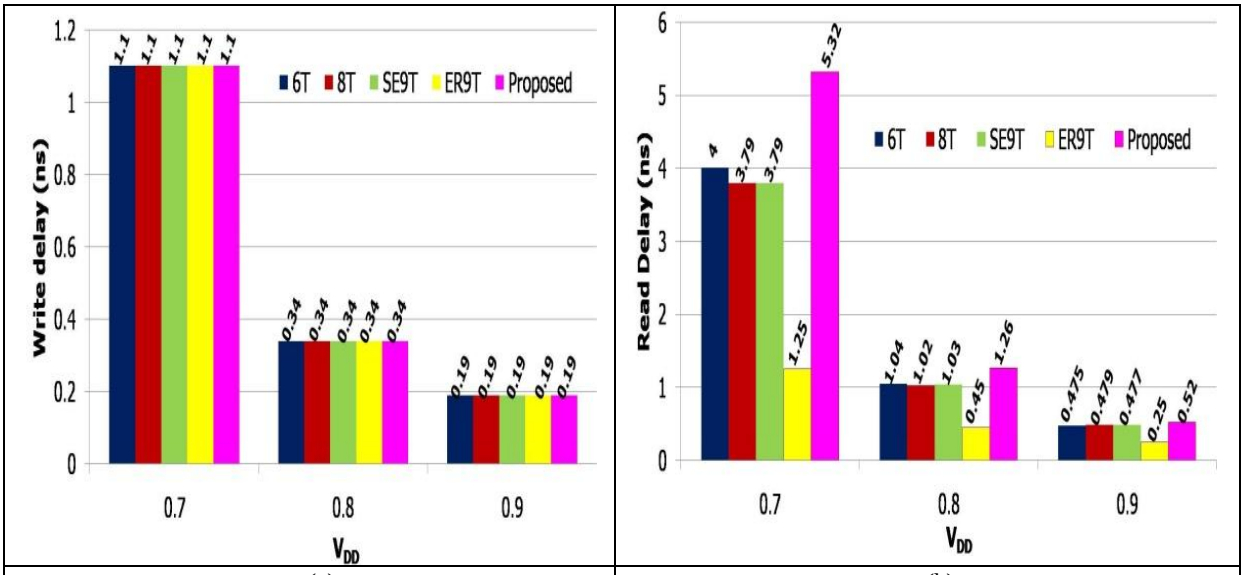


Fig. 4 Comparisons of (a) write delay and (b) read delay at different VDD

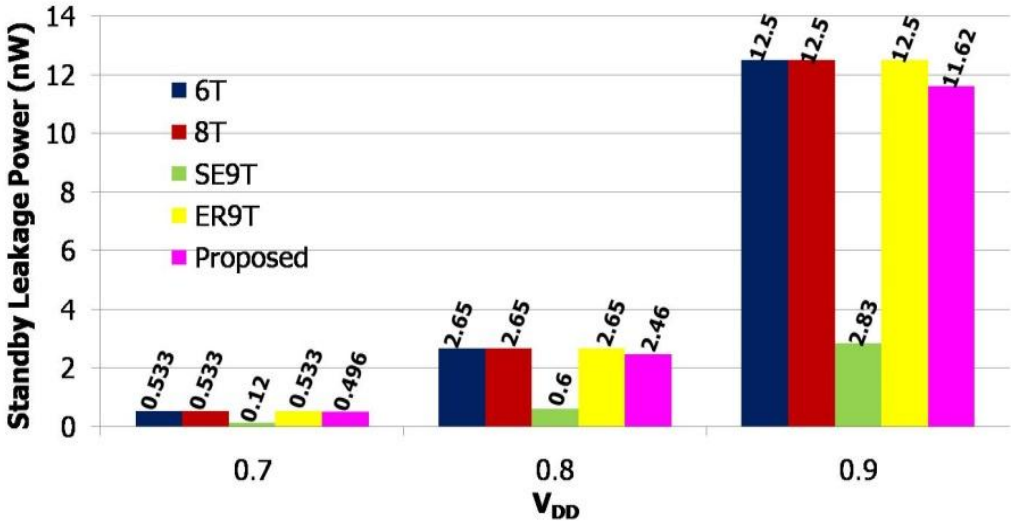


Fig. 5 Comparison of standby leakage power consumption at different VDD

IV. Conclusion

In this paper, we explored single ended read and differential write based 8T SRAM cell structure for enhanced WSNM and lower leakage power. This cell is based on 8T SRAM cell. Here, extra read word line controlled stack transistor is added to reduce the leakage power consumption. The comparative analysis was simulated using HSPICE at 22nm MOS technology at different voltage ranges from 0.7V to 0.9V. The simulation outcomes showed that the proposed cell had superior WSNM and leakage characteristics compared to 6T, 8T and ER9T. Also, our design offers similar layout area as 8T and ER9T.

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