ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 7, July 2016

REVIEW PAPER ON BINARY TO BCD CONVERTER FOR DECIMAL ADDER

Poornima Shrivastava [1], Prof. Balram Yadav [2]

[1,2] Scope College Of Engineering, Bhopal, India

Abstract-Decimal data processing applications have grown exponentially in recent years thereby increasing the need to have hardware support for decimal arithmetic. Binary to BCD conversion forms the basic building block of decimal digit adder. This paper presents novel high speed low power architecture for binary to BCD conversion which provides better results in terms of power, area, and delay than the existing designs of binary to BCD converter.

INDEX TERMS: -BCD adder, add-3 algorithm converter.

I. INTRODUCTION

The center of any kind of digital processor and micro processor is its data path. Data path is the one of the critical component which decides the key parameters of their design such as the clock frequency, area and power dissipation look up table of the design. Adders and multipliers are the foremost components in the data path and they are of major anxiety for the any digital designer of the data path. The use Of IP being popular for designing outsized systems, it is of more significance to consider the presentation of various digital adder and digital multiplier implementations that are offered with the commercially available IP. This paper is addressed on analyzing digital Adders and that are available to design with VHDL. Decimal data processing applications have matured exponentially in modern years thereby increasing the necessity to have hardware and software support for decimal arithmetic. Decimal Arithmetic is receiving noteworthy attention in marketable business and internet stand applications, providing hardware and software support and in this direction it is hereafter that necessary calculations done is of saleable, scientific and of financial use.

II. PROPOSED WORK

The first approach has a binary to BCD adder using a novel Double Digit Decimal Adder (DDDM) technique. Simultaneously a novel design for BCD digit adder that reduces the critical path and area is also presented in this thesis. The ripple adder has to be an efficient, high speed adder, less complexity to achieve high performance.

Adder Name	Complex (T)	Delay for n-bit
Ripple Carry Adder(RCA)	O(n)	2n

To approximate the propagation delay of this adder, we ought to look at the most awful case delay more than every possible combination of binary inputs. This is also known as the significant path. The most noteworthy sum bit can only be calculated when the carry out of the earlier FA is known. In the worst case (when all the carry out's are 1), this carry bit necessitate to ripple across the structure from the smallest amount significant arrangement to the most significant position. Figure 3.4 has a darkened line representative the decisive path. $T_{RCA\text{-}4bit}$ = T_{FA}(A0,B0→*C*o)+*T* FA (*C* in→*C*1)+

T_{FA} (*C*in→*C*2)+ T_{FA} (*C*in→*S*3) ……1.1

And, it is easy to extend to k-bit RCA:

$T_{RCA\text{-}4bit}$=T_{FA}(A0,B0→*C*o)+(*K*-2)*T_{FA} (*C*in→*C*i)+ T_{FA} (*C*in→S_{k-1}) ……1.2

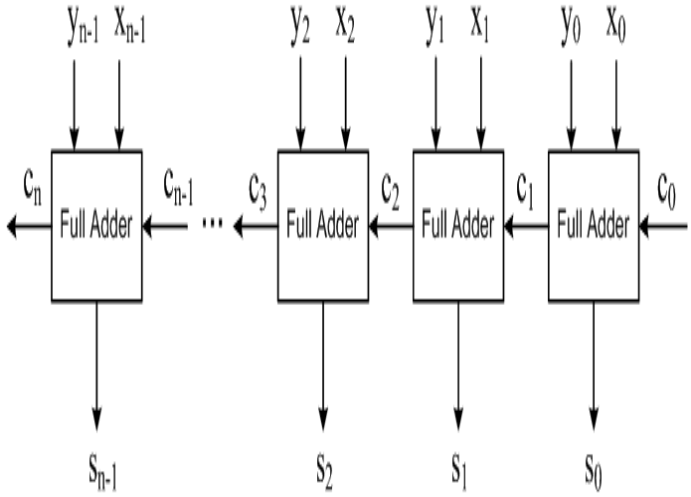

Figure 1.1 Schematic for an N-bit Ripple Carry Adder

Though the shift and add by 3 algorithm is not novel, the architecture implementation using add by constant which ultimately makes it area efficient is shown in figure 1.1.The main goal of proposed algorithm is to perform proficient fixed bit binary to BCD conversion.

The binary to BCD can be designed using iterative and add-3 approaches This paper presents two novel techniques for binary adder The main motive of the proposed algorithm is to execute significantly capable fixed bit binary to BCD conversion in terms of delay ,power and area.

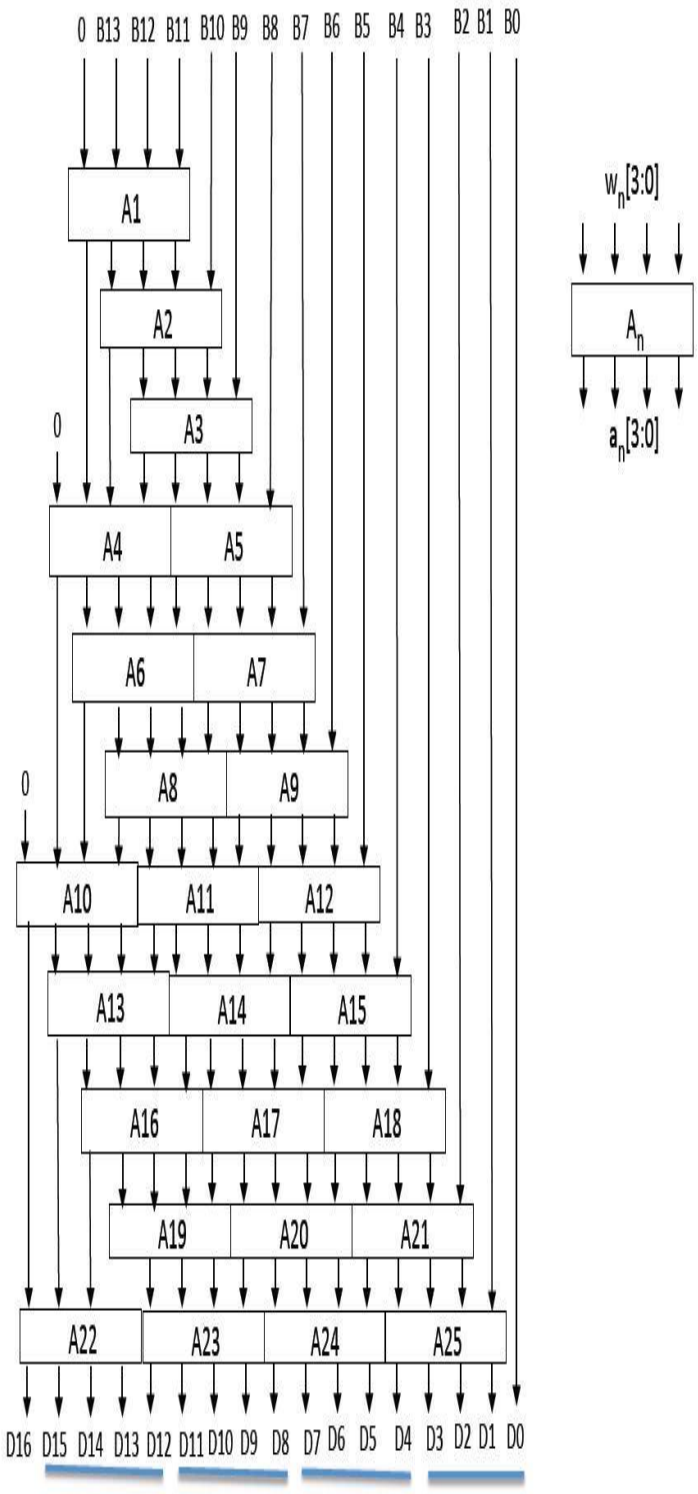

Figure 1.2: Proposed Shift add by constant Architectural Implementation

most of the newly proposed adder use 16-bit binary to BCD converters. The proposed algorithm has been intentionally designed for such converters. The following section explains the proposed algorithm used in this paper.

III. LITERATURE SURVEY

IEEE standard for floating-point arithmetic IEEE SC, Oct.2006 [1] .Here the focus is on the rising appreciation of decimal computer arithmetic in scientific, commercial, financial and Internet-based applications, the only hardware realization of decimal arithmetic algorithms is in advance more importance. Thus Hardware decimal arithmetic units now help as an essential part of some newly commercialized general purpose processors, on the other hand complex decimal arithmetic operations, such as multiplication, have been recognized by somewhat slow iterative hardware algorithms. Nevertheless, with the fast improvements in very large scale integration (VLSI) technology, semi- and fully parallel hardware decimal multiplication units are predictable to change shortly. The foremost representation for decimal digits is the binary-coded decimal (BCD) encoding. The BCD digit multiplier can help as the significant building block of a decimal multiplier, regardless of the degree of parallelism. A BCD-digit multiplier yields a two-BCD digit product from two input BCD digits. We make available a novel design for

the former, showing some benefits in BCD multiplier implementations. ISSN (Print)

Erle, M.A.; Schwarz, E.M.; Schulte, M.J ,17th IEEE Symposium on Computer Arithmetic, 2005 [2]. Here in this paper they have proposed that a BCD-digit multiplier can assist as the key building block of a decimal multiplier, regardless of the degree of parallelism. A BCD-digit multiplier creates a two-BCD digit product from two input BCD digits. We provide a Performing fast, efficient, binary-to-decimal conversion. With a modest amount of circuitry, an order of magnitude speed enhancement is achieved. This attainment deals a matchless benefit to general-purpose computers needing special hardware to interpret between binary and decimal numbering systems.

Jaberipur,Ghassem,Kaivani,Amir; Computers, IEEE Transactions on Volume 58, Issue 11, Nov. 2009 [9]. Here they described a serial binary/ decimal conversion algorithm, the BIDEC method. It was a two step method connecting a shift shadowed by a parallel modification of the data being converted. Now with the assistance of the integrated-circuit J-K flip-flop, the implementation of this two-step process needs an extreme amount of control logic. This paper presents a one-step conversion algorithm that is appropriate for binary-to-decimal and decimal-to-binary conversion. An all purpose design application of the one-step algorithm.

The advantages of this novel algorithm include low procedure for expressing the conversion registers as a present state/next-state counter problem is given, along with numerous samples of the cost, faster operation, and also hardware modularity.

Fast and compact binary-to-BCD conversion circuits for decimal multiplication ,Osama Al-Khaleel ,Jordan University of Science and Technology, Irbid, Jordan ; Zakaria Al-Qudah ; Mohammad Al-Khaleel ; Christos A. Papachristou Computer Design (ICCD), 2011. [13]. Here in this paper they have proposed that Decimal arithmetic has received considerable attention recently due to its suitability for many financial and commercial applications. In particular, numerous algorithms have been recently proposed for decimal multiplication. A major approach to decimal multiplication shaped by these proposals is based on performing the decimal digit-by-digit multiplication in binary, converting the binary partial product back to decimal, and then adding the decimal partial products as appropriate to form the final product in decimal. With this approach, the efficiency of binary-to-BCD partial product conversion is critical for the efficiency of the overall multiplication process. A recently proposed algorithm for this conversion is based on splitting the binary partial product into two parts (i.e., two groups of bits), and then computing the contributions of the two parts to the partial BCD

result in parallel. This paper proposes two new algorithms (Three-Four split and Four-Three split) based on this principle. We present our proposed architectures that implement these algorithms and compare them to existing algorithms. The synthesis results show that the Three-Four split algorithm runs 15%faster and occupies 26.1%less area than the best performing equivalent circuit found in the literature. Furthermore, the Four-Three split algorithm occupies 37.5% less area than the state of the art equivalent circuit.

FPGA Implementation of Low Power Hardware Efficient Flagged Binary Coded Decimal Adder K.N.Vijeya kumar V. Sumathy Assistant Professor, Ece, Assistant Professor, Ece, Anna University Of Technology, Government College Of Technology, Coimbatore [14]. This paper presents a novel architecture for hardware efficient binary represented decimal addition. We extend the two operand ripple carry addition by one with the third input being constant. The addition technique is made fast by generating flag bits appropriate to the constant added. The third constant in case of our proposed design is 6(0110) for converting the outputs exceeding 9 to Binary Coded Decimal (BCD) number. The proposed BCD adder has been designed using VHDL code and synthesized using Altera Quartus II. Experimental results show that the proposed design outperforms the previous researches in terms of power dissipation and area.

A High Performance Binary to BCD Converter, A. Hari Priya1 Assistant Professor, Dept. of ECE, Indur Institute of Engineering. and Technology, Siddipet, Medak, India [15]. Here they have proposed that the Decimal data processing applications have grown exponentially in recent years thereby increasing the need to have hardware support for decimal arithmetic. Binary to BCD conversion forms the basic building block of decimal digit multipliers. This paper presents novel high speed low power architecture for fixed bit binary to BCD conversion which is at least 28% better in terms of power-delay product than the existing designs. 8.

IV. CONCLUSIONS

A Novel integrated BCD/ Binary multi-operand addition algorithm. The binary parallel multi-operand addition is to be used by programmers to convert a binary number to decimal. It will be performed by shift and add by 3 algorithms, and can be implemented by using a less number of gates in computer hardware, which ultimately makes it area efficient.

V. REFERENCES

[1] IEEE standard for floating-point arithmetic. IEEE SC, Oct. 2006 at http://754r.ucbtest.org/drafts/754r.pdf

[2] Erle, M.A.; Schwarz, E.M.; Schulte, M.J., "Decimal multiplication with efficient partial product generation," 17th IEEE Symposium on Computer Arithmetic, 2005. ARITH-17 2005, 27-29 June 2005, pages21-28.

[3] Erle, M.A.; Schulte, M.J., "Decimal multiplication via carrysave addition," Proceedings. IEEE International Conference on Application-Specific Systems, Architectures, and Processors, 2003, 24-26 June, 2003 Page(s):348 - 358.

[4] A; Antelo, E M"i Vazquez A; Antelo, E; Montuschi P, "A New Family of High-Performance Parallel Decimal Multipliers" in the 18th IEEE Symposium on Computer Arithmetic 25-27 June 2007.

[5] Sreehari Veeramachaneni, M. Keerthi Krishna , L. Avinesh, P Sreekanth Reddy, M.B. Srinivas, "Novel High-Speed 16-Digit BCD Adders Conforming to IEEE 754r Format", IEEE Computer Society Annual Symposium on VLSI (ISVLSI‟07), pages 343-350, Mar 2007.

[6] Decimal multiplication using compact BCD multiplier James, R.K.; Shahana, T.K.; Jacob, K.P.; Sasi, S.; Electronic Design, 2008. ICED 2008. International Conference on 1-3 Dec. 2008 Page(s):1 – 6.

[7] Binary-coded decimal digit multipliers Jaberipur, G.; Kaivani, A. Computers and Digital Techniques, IET Volume 1, Issue 4, July 2007 Page(s):377 - 381.

[8] Novel High-Speed Architecture for 32-Bit Binary Coded Decimal (BCD) Multiplier Veeramachaneni, S.; Srinivas, M.B. Communications and Information Technologies, 2008. ISCIT 2008. International Symposium on 21-23 Oct. 2008 Page(s):543 – 546

[9] Improving the Speed of Parallel Decimal Multiplication Jaberipur, Ghassem; Kaivani, Amir; Computers, IEEE Transactions on Volume 58, Issue 11, Nov. 2009 Page(s):1539 - 1552.

[10] Schmookler, M.: „High-speed binary-to-decimal conversion‟, IEEETrans. Comput., 1968, 17, (5), pages. 506–508.

[11] Rhyne, V.T.: „Serial binary-to-decimal and decimal-to-binary conversion‟, IEEE Trans. Comput., 1970, 19, (9), pages. 808– 812.

[12] Arazi, B., and Naccache, D.: „Binary-to-decimal conversion based on the 28 2 1 by 5‟, Electron. Lett., 1992, 28, (23), pages. 2151–215

[13] Fast and compact binary-to-BCD conversion circuits for decimal multiplication Osama Al-Khaleel ; Jordan University of Science and Technology, Irbid, Jordan ; Zakaria Al-Qudah ; Mohammad Al-Khaleel ; Christos A. Papachristou Computer Design (ICCD), 2011

[14] FPGA Implementation of Low Power Hardware Efficient Flagged Binary Coded Decimal Adder

K.N.Vijeyakumar V.Sumathy Assistant Professor, Ece, Assistant Professor, Ece, Anna University Of Technology, Government College Of Technology, Coimbatore, Coimbatore - 641047. Thadagam Road, Coimbatore-641013.

[15] A High Performance Binary to BCD Converter A. Hari Priya1 Assistant Professor, Dept. of ECE, Indur Institute of Engineering. and Technology, Siddipet, Medak, India 1