ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 7, July 2016

FAST AND LOW POWER DISSIPATION BINARY TO BCD CONVERTER FOR MULTI-OPERAND B/D ADDER

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Abstract- In view of increasing eminence of commercial, economic and Internet-based applications that process data in decimal arrangement, Synthesis results for 2, 4, 8, and 12 operands and 8 decimal digits provide useful statistic in formative each adder's performance and scalability. There is a renewed interest in providing hardware support to handle decimal data. In this paper, a new architecture decimal addition of binary coded decimal (BCD) operands, which is the core of high speed multi-operand adders and ,is proposed Simulation results show that the proposed add-3 digit BCD adder achieves an improvement of 40% in delay. The 2,4,8,16-digit BCD look-ahead adder shown to achieve at least 70% faster than the obtainable ripple carry one.

INDEX TERMS:- BCD adder, add-3 algorithm, binary to BCD convertor, decimal arithmetic.

I. INTRODUCTION

Utilization of binary data is very speedy on digital computers. But seeing as, decimal arithmetic is more beneficial than binary Arithmetic operation; the conversion of binary data to BCD data is involved. Decimal multiplication is the fundamental operation for any hardware implementation of decimal arithmetic and it is also a fundamental part to the above mentioned digital decimal-dominant applications Decimal Arithmetic is receiving significant attention in commercial business and internet based applications, providing hardware support in this direction is henceforth necessary. Improving BCD architectures, to enable faster and compact arithmetic. In this paper we introduce a new architecture for binary to BCD Conversion of partial products which forms the core of decimal multiplication algorithms such as [7] and [8]. The speedup, area reduction and power consumption of the proposed architecture is analyzed and comparisons with recent architectures is provided. The current state of art conversion scheme [7] is studied and irregularities in the implementation of their converter have been discussed.

The Results show that the proposed design brings considerable improvement in terms of latency, area and power consumption overview on general BCD conversion and its need.

The binary numbering system is, far-off the most ordinary numbering system in use in computer systems in this scenario. In days Because of there were all the computer systems that were based on the decimal numbering

system slightly than the binary numbering system. Such computer systems were very well-liked in systems generally or for business/commercial systems. And internet based applications, even though systems designers have realize that binary arithmetic is not quite always better than decimal arithmetic for general calculation and application the parable still continue that decimal arithmetic is better for money calculations and some general purpose application than binary arithmetic. as a result, many software systems still identify the use of decimal arithmetic in their calculations [16].BCD demonstration does offer one big advantage over binary representation: it is practically small to convert between the string representation of a decimal number and its BCD representation. This feature is for the most part valuable when working with fractional values since fixed and floating point binary representations cannot exactly represent many

II. RELATED WOR

Shift the binary number left one bit. 2. If 8 shifts have taken place, the BCD number is in the Hundreds, Tens, and Units column. 3.

Operation	Tens	Units	Binary
HEX			E
Start			1 1 1 0
Shift 1		1	1 1 0
Shift 2		1 1	1 0
Shift 3		1 1 1	0
Add 3		1 0 1 0	0
Shift 4	1	0 1 0 0	
BCD	1	4	

If the binary value in any of the BCD columns i

5 or greater, add 3 to that value in that B column

4. Go to 1.table 1 show how to take bit and shift into hundred , units ,tens column Table shown how to shift bit .fig. 1 shown the flow chart of 16 bit binary to BCD converter if 8 shifts have taken place, the BCD number is in the Hundreds, Tens, and Units column.3. If the binary value in any of the BCD columns is 4 or greater, add 3 to that value in that BCD column.

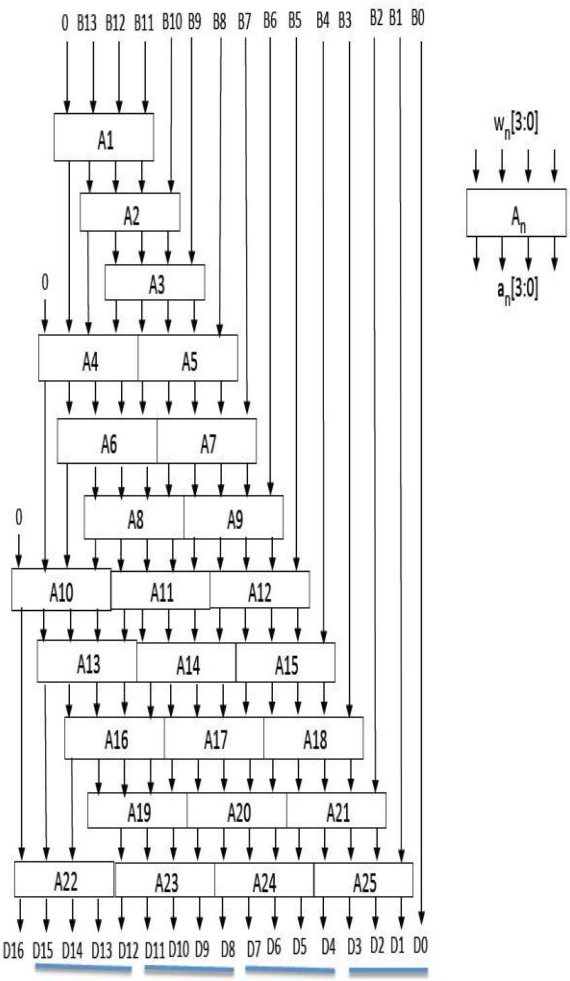

Fig.1 Basic block of 16bit add3 conversion

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III. PROPOSED ALGORITHM

The algorithm then iterates *n* times. On each and every iteration, the complete scuff space is left-shifted one bit. Though, before the left-shift is done, any BCD digit which is greater than 4 is incremented by 3. The increment make certain so as to a value of 4, incremented and left-shifted, revolve out to be 16, thus correctly "carrying" into the next BCD digit, This algorithm is convention but proposed architecture combine each BCD bits also overcome the area necessitate and get improve speed as conservative adder .The following subsection explains the proposed algorithm. The algorithm then iterates *n* times. On each iteration, the entire scratch space is left-shifted one bit. However, before the left-shift is done, any BCD digit which is greater than 4 is incremented by 3. Shown in fig.2

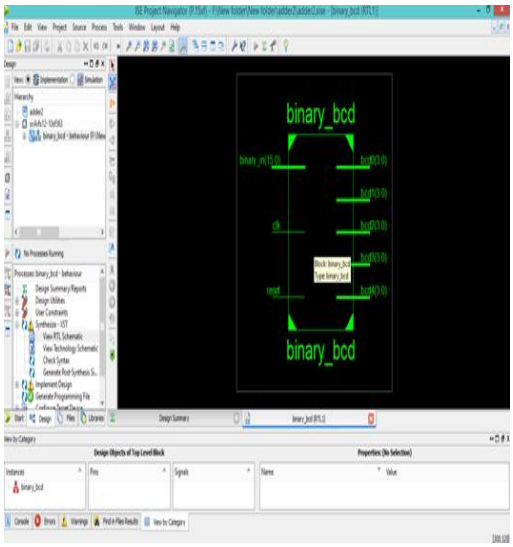

Fig.2 Shown the Input Output RTL view of 16bit

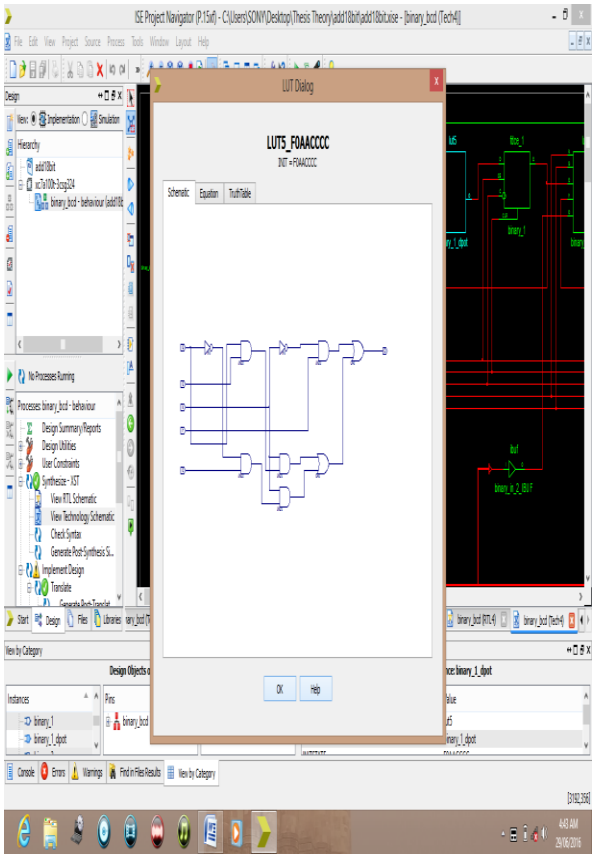

Fig.3 Shown the LUT view of 16bit Binary to BCD converter

The algorithm then iterates *n* times. On each and every iteration, the intact graze space is left-shifted one bit. However, before the left-shift is done, any BCD digit which is greater than 4 is incremented by 3. The increment ensures that a value of 4, incremented and left-shifted, becomes 16 thus correctly "carrying" into the next BCD digit. this algorithm is tradition but proposed architecture amalgamate each BCD bits also conquer the area required and get enhanced speed as conventional adder fig.3 shown RTL view of synthesize 16 bit BCD to binary code .

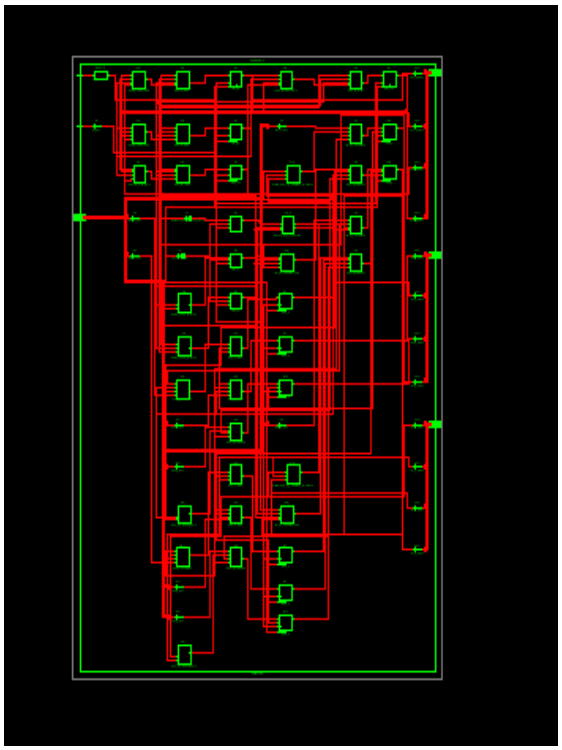

Fig.4 RTL view of 16bit Binary to BCD conversion

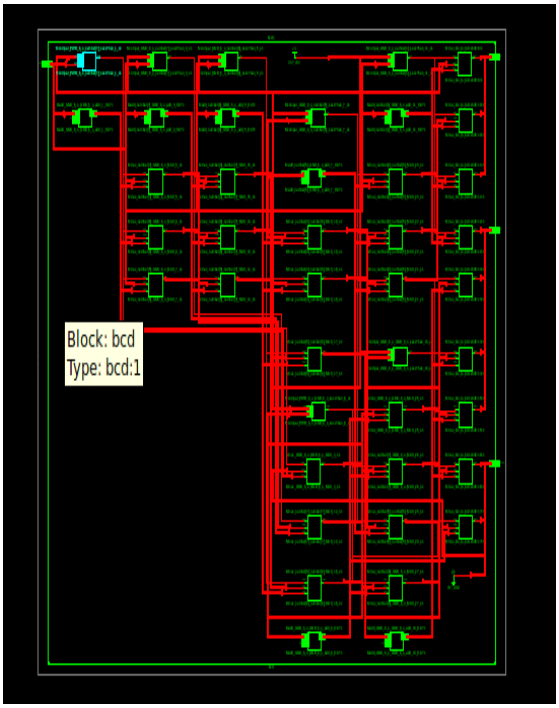

Fig.5 RTL view of 16bit Binary to BCD conversion

IV.BINARY TO BCD CONVERTER

All the 16 -bit Binary to BCD converters and add and shift structures were described using VHDL data flow modeling and simulated using Simulator (Isim) 14.7. The Binary to BCD converters and Multi-operand designs were mapped on, RTL Compiler on 14.7(Isim). All the inputs were set to have a clock rate of 100%. Binary to BCD structures based on the proposed algorithm were designed and the Binary to BCD converter in the proposed algorithm was replaced with that of architecture [8] for fair comparisons. Table 1 shows the comparison of Binary to BCD converter with existing design [1]. Synthesis results show that there is a reduction in delay by 55 % with a tradeoff in power by 18 %. This in turn reduces power delay by 27 % and Total REAL time to Xst completion: 1.00 sec. Total CPU time to Xst completion:0.10 and Maximum combinational path delay: 2.710ns secs from these three designs, the proposed multi-operand adder in concurrence with modified binary to BCD adder using add-3 [3] gives better performance in terms speed as well as power –delay product. Further it is evident from Table-I that the proposed design performs better compared to [4] with respect to delay as well as power delay product

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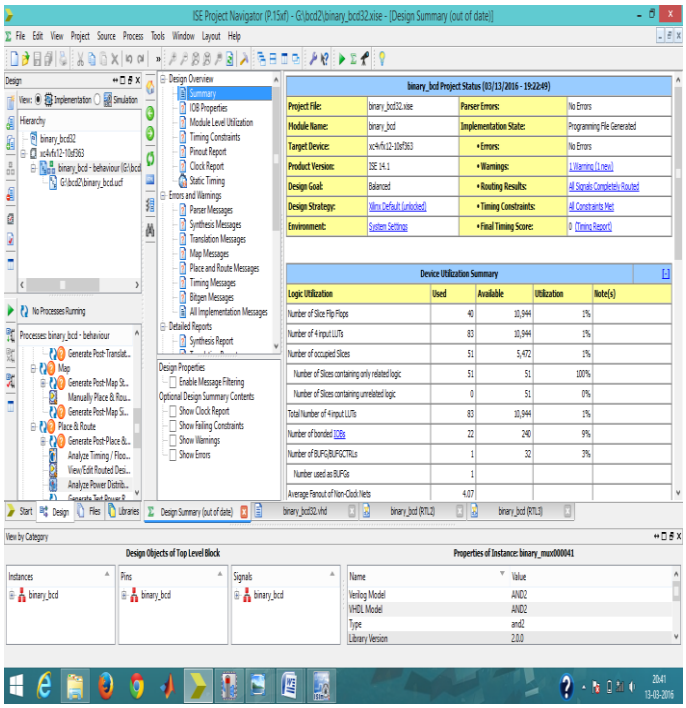

Fig.6 Design summary of the proposed Design

Metric	Area (μm2)	Delay (ns)	Power (w)	Metric
Proposed design	48 LUT used of 63,400 Utilization 1%	1.663	0.42	Proposed design
Design [1]	903	1.89	549	Design [1]

TABLE I .Comparison of Proposed add 3 Adder With customized hundred and units and tens– Four Split [8] Adders

V. SIMULATION RESULTS

All the 16 -bit Binary to BCD converters and Multi operand adder structures were described using VHDL data flow modeling and simulated using Simulator (Isim) 14.7. The Binary to BCD converters and Multi-operand designs all the inputs were set to have a clock rate of 100%. Binary to BCD structures based on the proposed algorithm were designed and the Binary to BCD converter in the proposed algorithm was replaced with that of architecture [8] for fair comparisons. Table I shows the comparison of Binary to BCD converter with existing design [1]. Synthesis results show that there is a reduction in delay, power and area. This in turn reduces power delay product and Minimum period: 2.600ns (Maximum Frequency: 384.645MHz) & Minimum input arrival time before clock: 2.765ns & Maximum output required time after clock: 4.714ns Maximum combinational path delay: No path found

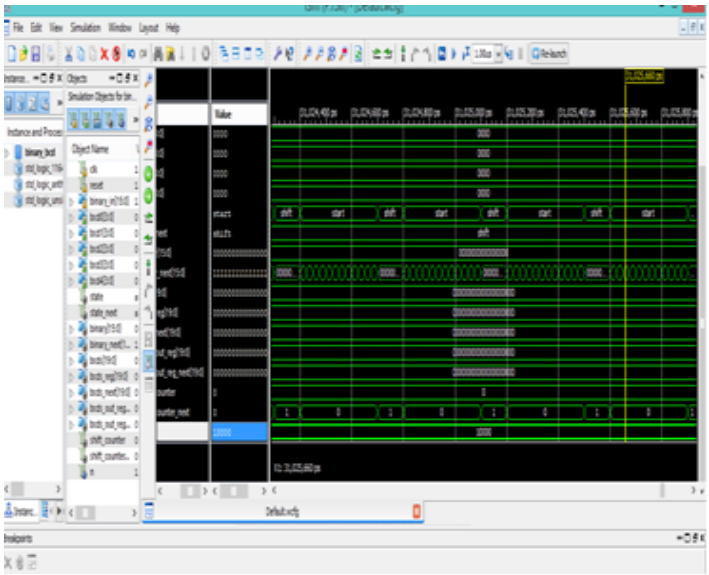

FIG.7 Simulation result of 16 bit Binary to BCD converter

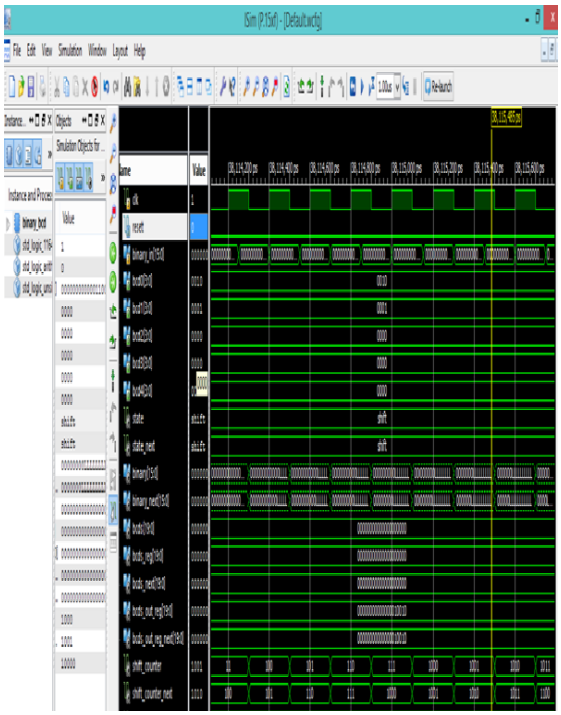

FIG.8 Simulation result of 16bit Binary to BCD converter

VI. CONCLUSIONS

A Novel integrated BCD/ Binary multi-operand addition algorithm has been proposed. The binary parallel multi-operand addition is realized using by programmers to convert a binary number to decimal. It is performed by shift and add by 3 algorithm, and can be implemented using a less number of gates in computer hardware, which ultimately makes it area efficient,. The proposed binary to BCD converter forms the core of the multi-operand binary adder. Simulation results show the efficiency of our Proposed BD converter in addition to multi-operand decimal adder with respect to exiting designs.[10]

VII. REFERENCES

1. [1] Area-Efficient and Power-Efficient Binary to BCD Converters Sri Rathan Rangisetti, Ashish Joshi, Tooraj Nikoubin, Member, IEEE Dept. of Electrical & Computer Engineering, Texas Tech University, Lubbock, TX, 79409

2. [2] M. D. Ercegovac and T. Lang, Digital Computer Arithmetic. Elsevier/Morgan Kaufmann Publishers,2004.

3. [3] R. D. Kenney and M. J. Schulte. High-speed multi-operand decimal adders. IEEE Trans. on Computers, 54(8):953–963,Aug.2005

4. [4] Dadda, Luigi. "Multi-operand parallel decimal adder: A mixed binary and bcd approach." Computers, IEEE Transactions on 56.10 (2007): 1320-1328.

5. [5] Lin, Kuan Jen, et al. "A parallel decimal adder with carry correction during binary accumulation." New Circuits and Systems

6. Conference (NEWCAS), 2012 IEEE 10th International. IEEE, 2012.

7. [6]- Jaberipur,Ghassem, and Amir Kaivani. "Improving the speed of parallel decimal multiplication." Computers, IEEE Transactions on 58.11 (2009): 1539-1552.

8. [7]- Bhattacharya, Jairaj, Aman Gupta, and Anshul Singh. "A high performance binary to BCD converter for decimal multiplication." VLSI Design Automation and Test (VLSI-DAT), 2010 International

9. Symposium on. IEEE, 2010.

10. [8]- Al-Khaleel, Osama, et al. "Fast and compact binary-to-BCD conversion circuits for decimal multiplication." Computer Design (ICCD), 2011 IEEE 29th International Conference on. IEEE, 2011.

11. [9] S. Knowles, ‘‘A family of adders,’’ in: Proceedings of the 14th IEEE Symposium on Computer Arithmetic, pp. 30–34, 1999-368

12. [10] A Decimal / Binary Multi-operand Adder using a Fast Binary to Decimal Conver2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems
13. Ranaganathan Panchagam “Minimization of Power Dissipation in Digital Circuits Using Pipelining and a Study of Clock Gating Technique” Master’s Thesis,