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SIMILARITY ORIENTED LOGIC SIMPLIFICATION BETWEEN UNIPOLAR RETURN TO ZERO AND MANCHESTER CODES

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***Abstract*:** The line codes are used for variety of applications. The code diversity between Unipolar and Manchester code seriously limits the potential to design a fully reused VLSI architecture.The combined architecture of both Manchester and unipolar RZ codes can be used for optical fiber communication and dedicated short range communications. In this paper, similarity oriented logic simplification is used to exploits the characteristics of two codes and design a fully reused VLSI architecture .This results can be used in various applications. The result shows that sols technique improves the hardware utilization ratio.SOLS improves hardware utilization ratio from 55% to 57%.

Key words-Dedicated short range communication, Unipolar, Manchester,VLSI

I. INTRODUCTION

The line codes are used to transmit the binary data. The first approach converts digital data to digital signal, known as line coding; Line coding techniques can be broadly divided into three broad categories: Unipolar, Polar and Bipolar. In Unipolar encoding technique, only two voltage levels are used. It uses only one polarity of voltage level. In this encoding approach, the bit rate same as data rate. Polar encoding technique uses two voltage levels ,one positive and the other one negative. In Bipolar encoding techniques zero level is used to transmit the binary 0 and binary 1 is represented by alternative positive and negative voltages[3].

There are two formats are used to transmit the Unipolar or polar data, they are non return to zero and return to zero formats. Non return to zero format, is the most common and easiest way to transmit digital signals and it use two different voltage levels for the two binary digits. Usually a negative voltage is used to represent one binary value and a positive voltage to represent the other. The data is encoded as the presence or absence of a signal transition at the beginning of the bit time. In NRZ encoding, the signal level remains same throughout the bit-period. In this format most of the energy is concentrated between 0 and half the bit rate [1], [2],[3].

The advantages of NRZ is Detecting a transition in presence of noise is more reliable than to compare a value to a threshold and NRZ codes are easy to engineer and it makes efficient use of bandwidth. The main limitations of NRZ are the presence of a dc component and the lack of

synchronization capability. When there is long sequence of 0's or 1's, the receiving side will fail to regenerate the clock and synchronization between the transmitter and receiver clocks will fail. The return to zero format provide synchronization, here a signal transition occurs in each bit .The required transition occur for half of the time period and the value is return to zero for next half bit duration. Key characteristics of the RZ coding are, it has no dc component, good synchronization and the Main limitation is the increase in bandwidth [3].

Nowadays Power is a major problem faced by all electronics and electrical circuits. The main objective of this work is to combine the VLSI architecture of Unipolar RZ and Manchester encoding so that it reduces the power used, by reducing the total number of components and improves the performance of both codes. The main application of line codes are in systems like dedicated short range communication. The DSRC is briefly classified in to two broad categories that are automobile to automobile and automobile to road side. The DSRC enables the message sending and broadcasting among automobiles for safety issues and public information announcement [2, 4, 6, 10].

The automobile to road side focuses on intelligent transportation service. Normally FM0 coding and Manchester coding is used for signal transmission. We can also use Unipolar and Manchester code for signal transmission. The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain DC-balance. The purpose of Unipolar and Manchester code is to provide the transmitted signal with DC balance [1], [2].

II. SYSTEM DESIGN

The coding principles of Manchester and Unipolar RZ codes are discussed as follows.

A. Manchester Encoding

Manchester encoding is also called phase encoding. it can be used for higher operating frequency. Manchester encoding is very common method and is probably the most commonly used. In Manchester encoding the average power is always the same, no matter what data is transmitted. The codes always produce a transition at the center of bit.

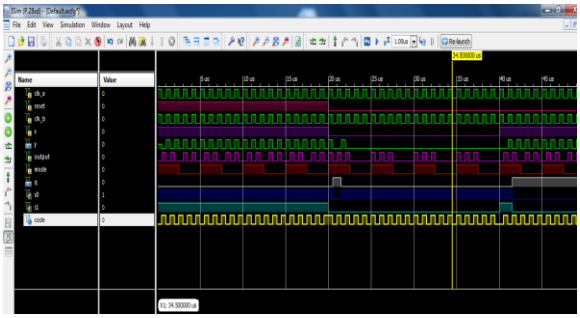

Fig.1 Manchester code

Here logic '1' is represented by transition from HIGH to LOW. Logic '0' is represented by transition from LOW to HIGH. The operation of Manchester coder is an exclusive OR of the input signal with clock signal.

B. Unipolar Return to zero Encoding

Unipolar Return to zero code has single polarity. The transmission rules for Unipolar RZ is

- For input '0', a '0' is transmitted for the entire duration of clock period
- For input '1', a high polarity is transmitted for half bit duration and return to state '0' for next half bit duration [3].

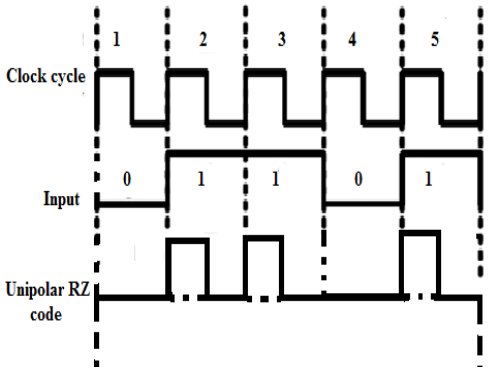

Fig 2. Unipolar RZ code

c. Analysis of two codes

The Manchester code can be easily realized using X-OR gate. From the figure of unipolar code, we can derive the FSM of the code. It is shown below,

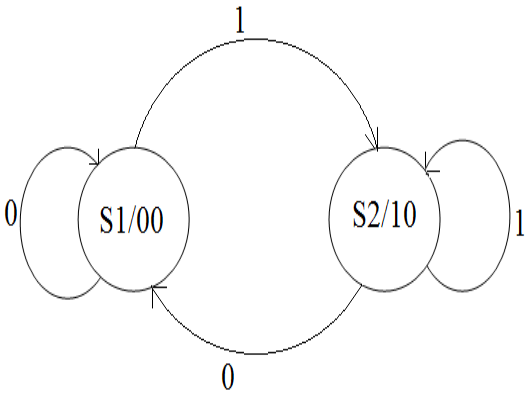

Fig.3 FSM of Unipolar RZ code

We are here using Moore machine modelling,the output depends on the present state, when the input is at logic '0' machine is in state S_1 with output "00".When input is at logic '1'in state S_1 the state changes to S_2 With output "10".In state S_2 when the input is at logic '1',machine remains in state S_2 with output "10".when the input is at logic '0',machine goes to state S_1 here output is "00".From FSM we can develop transition table[7].

Present state	Next state	
	Input = 0	Input = 1
S1	S1	S2
S2	S1	S2

TABLE 1.Transition table of Unipolar code

We are assigning state code to each state and each state consists of A and Here A(t) and B(t) represent the discrete time state code of current state at time instant t.Their previous states are denoted by A(t-1) and B(t-1) respectively.

Present state		Next state			
A(t)	B(t)	Input = 0		Input = 1	
		A(t)	B(t)	A(t)	B(t)
0	0	0	0	1	0
1	0	0	0	1	0

TABLE 2.State table of unipolar code

By solving for A(t) and B(t) in terms of A(t-1) ,B(t-1) and input X we get,

$$A(t) = X \text{ AND } (\text{NOT } B(t-1)) \quad (1)$$

$$B(t) = \text{NOT } B(t-1) \quad (2)$$

From (1) and (2) we can design the architecture for combined unipolar and Manchester codes it is shown in Fig.4.

The hardware architecture for Unipolar RZ and Manchester code consists of separate logic for Unipolar RZ

code and Manchester code. The Manchester code can be realized using a simple EX-OR gate. Manchester code is the result of EX-OR operation of input with clock. The logic for Unipolar RZ consists of two D flip flops, multiplexer ,AND gate and data selector.

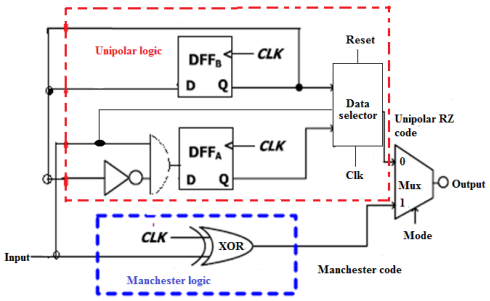

Fig.4. Hardware architecture of Unipolar RZ code and Manchester code

The D flip flops are used to store the state codes of Unipolar code.The effect is that D input condition is only copied to the output Q when the clock input is active. The D flip flop will store and output whatever logic level is applied to its data terminal so long as the clock input is HIGH. The output of DFFB is feedback to the input of DFFB. On the next negative edge of clock pulse applied to the DFFB ,the present value at the input of FF is passed to the output of FF.The DFFA is used to implement the logic for A(t),the inverted output of FFB and the input is given as the input of the DFFB.

The outputs of both DFFA, DFFB, input, clock and reset is given to the data selector. The data selector selects the correct output (either the output of DFFA or the output of DFFB) as its output. Depending on the conditions on the clock, input and reset, data selector switches between outputs of DFFA and DFFB.The output of the data selector produces the Unipolar RZ code. A multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line.

A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. Multiplexers can also be used to implement Boolean functions of multiple variables. Here we are using a 2:1 multiplexer, the inputs to the multiplexer are Unipolar RZ and Manchester code. The multiplexer is used to switch between unipolar code and Manchester code depending on the mode signal. When mode=0, unipolar code is selected and when mode=1 Manchester code is selected. The clock signals applied to the all components of the circuit are of equal time period otherwise loss of data occurs[7].

C. Hardware Utilization Ratio

HUR is defined as the ratio of active components to the total component in percentage. The component is defined as hardware to perform a specific logic function. The active components mean the components present in both codes. Total components are the number of components in entire architecture. The total transistor count can be calculated by counting the transistors used to implement the components used in the circuit. The HUR for the above circuit is shown below,

Coding	Active components(transistor count)/Total components(transistor count)	HUR
Manchester code	2 (42) / 7 (170)	24.70%
Unipolar code	6 (148) / 7(170)	87.05%
Average	4 (95) / 7 (170)	55.88%

TABLE 3.HUR of circuit

For the Manchester code EX-OR gate and multiplexer are the active components and for Unipolar RZ code the two flipflops, AND gate, NOT gate, data selector and

the multiplexer are active components. From the table, we can see that on an average the above circuit uses four components among the seven components .Our aim is to increase the HUR

III. VLSI ARCHITECTURE BASED ON SOLS

The SOLS technique is divided into area compact retiming and balance logic sharing.

A. Area compact retiming

The state code is stored in DFFA and DFFB.Logic for A(t)and B(t) consists of gates. Data selector produces unipolar RZ code depending on the inputs. From expressions (1) and (2) we can see that A(t) and B(t) is only depends on B(t-1).From this we can conclude that only B(t-1) is needed to store, this require only one flipflop i.e. DFFB. We can eliminate the D flipflop needed to store state code for the logic A(t).

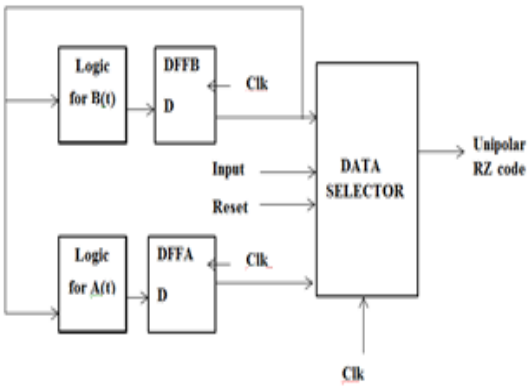

Fig.5Unipolar code without area compact retiming

If DFFA is directly removed a non synchronization between A(t) and B(t) causes a logic fault in the circuit. To avoid this DFFB is relocated right after the data selector.

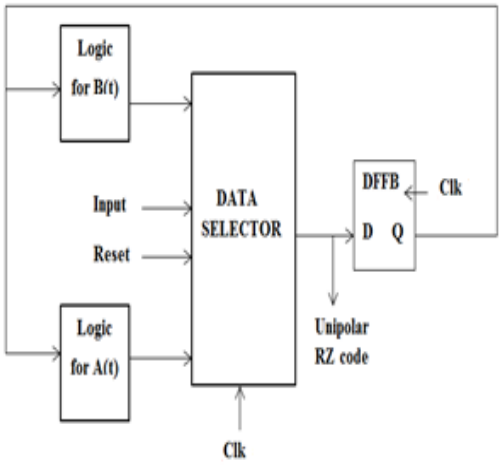

Fig .6. Unipolar code with area compact retiming

B.Balance logic operation sharing

The idea is to analyze both codes and combine the codes if possible and make the architecture less complex. The Unipolar and Manchester codes are analyzed and it shows that we cannot combine these codes any more. From these results the circuit is modified in to figure below,

The system consists of a multiplexer flip flop (DFFB), data selector, AND gate, NOT gate and EX-OR gate. Here the D flip flop is relocated after the data selector. The output of dataselector is Unipolar code and the output is fed to D flip flop. The output of D flip flop is fed backed to both inputs of data selector.

Initially the DFFB is cleared by the application of Reset signal and corresponding output make changes in the output of data selector. The logic for A (t) and B (t) is selected by the conditions on the inputs of dataselector.The corresponding value at the output of data selector is loaded in to the D flip flop at the falling edge of clock pulse applied at the D flip flop and corresponding output of D flip flop is generated and fed backed to the inputs of data selector.

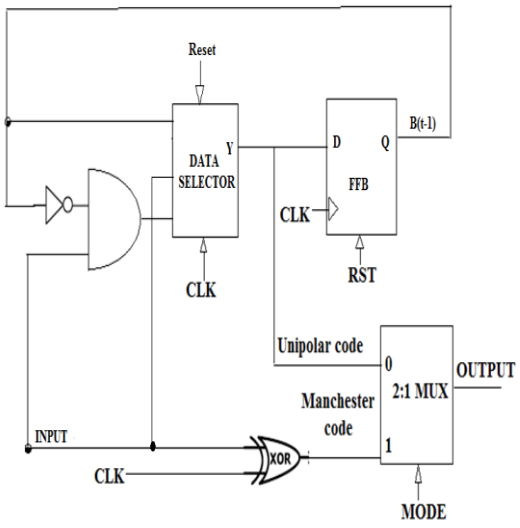

Fig .7. Modified hardware architecture for codes

The Unipolar code is alternatively switched between A(t) and B(t) through the data selector. When clock is at logic 0 the B(t) is passed through the data selector and this value is loaded in to DFFB at falling edge of clock pulse. When clock is at logic 1, the logic for A(t) is selected and the value is loaded in DFFB at falling edge of clock pulse. The alternative A(t) and B(t) generates the unipolar return to zero code. The unipolar RZ code and Manchester code is selected by the multiplexer through the mode signal.

C.HUR

The hardware utilization ratio of the modified circuit is shown below,

Code	Active component(Transistor count)/Total component(Transistor count)	HUR
Manchester code	2 (42) / 6 (144)	29.16%
Unipolar RZ code	5 (122) / 6 (144)	84.72%
Average	3.5 (82) / 6 (144)	57%

TABLE.4 HUR of modified circuit

From table we can see that the average HUR is increased from 55% to 57% and here the total numbers of transistors are reduced from 170 to 144.The HUR for Manchester code is also increased from 25% to 30% but in the case Unipolar code the HUR for the modified circuit is decreased to 85% from 87%. The modified circuit increases the hardware utilization and improves the circuit.

IV. EXPERIMENT RESULT AND DISCUSSION

The system is implemented using Xilink ISE Design Suite 14.2. using VHDL language. The Xilinx® ISE Simulator (ISim) is a Hardware Description Language (HDL) simulator that enables you to perform functional and timing simulations for VHDL, Verilog and mixed language designs.The ISE design suit 14.2 supports the devices like Kintex-7 325T,Kintex-7 410T, Virtex®-7 X485T.Performance increase of ~3.5% for the -2 speed grades for Kintex-7 and Virtex-7 FPGAs.

VHDL Language

VHDL (VHSIC Hardware Description Language) is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits. VHDL can also be used as a general purpose parallel programming language.

VHDL is commonly used to write text models that describe a logic circuit. Such a model is processed by a synthesis program, only if it is part of the logic design. A simulation program is used to test the logic design using simulation models to represent the logic circuits that interface to the design. This collection of simulation models is commonly called a testbench. VHDL is strongly typed and is not case sensitive. When a VHDL model is translated into the "gates and wires" that are mapped onto a programmable logic device such as a CPLD or FPGA, then it is the actual hardware being configured, rather than the VHDL code being "executed" as if on some form of a processor chip.

The key advantage of VHDL, when used for systems design, is that it allows the behaviour of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires).Another benefit is that VHDL allows the description of a concurrent system. VHDL is a dataflow language, unlike procedural computing languages such as BASIC, C, and assembly code, which all run sequentially, one instruction at a time.

A VHDL project is multipurpose. Being created once, a calculation block can be used in many other projects. However, many formational and functional block parameters can be tuned (capacity parameters, memory size, element base, block composition and interconnection structure).A VHDL project is portable. Being created for one element base, a computing device project can be ported on another element base, for example VLSI with various technologies[7].

Each component like D flipflop, Dataselector, Multiplexer, AND gate and X-OR gate is implemented in behavioral and data flow modeling. The combined code for both Unipolar RZ and Manchester code is done in structural modeling.

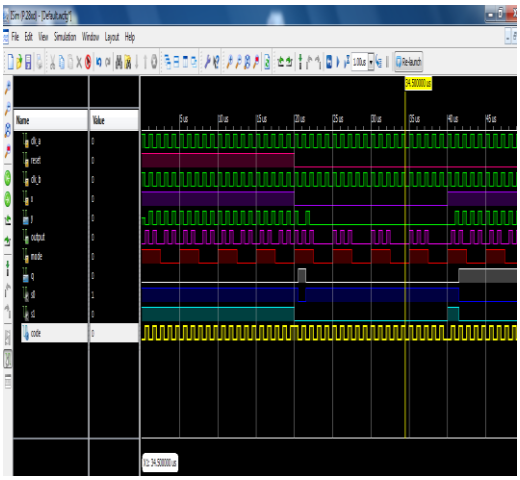

Fig.8. combined output

The Fig.8 shows the input sequence 1011, from result we can see that there exists one clock cycle delay between transition from logic 0 to logic 1 and vice versa. The mode signal is used to select Manchester or FM0 return to zero code. Here for input ‘1’ the clock is transmitted as code and for input ‘0’ the zero value is transmitted for Unipolar return to zero code. The Unipolar RZ code has no dc component, good synchronization. The RZ codes are primarily used in optical communication because it minimizes the power consumption and the effects of the system dispersion on optical signal distortion.

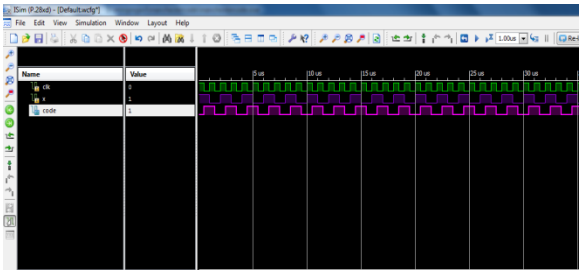

Fig.9 Manchester code

For Manchester code, the Fig.9 shows that the code is obtained by EXOR operation of the input sequence with clock cycle.

The RTL view of the system provides idea about the number of components and interconnections between them. The RTL consists of multiplexer, D flip flop, Manchester, NOT gate and AND gate. RTL design lies between a purely behavioral description of the desired circuit and a purely structural one. An RTL description describes a circuit's registers and the sequence of transfers between these registers but does not describe the hardware used to carry out these operations[8].

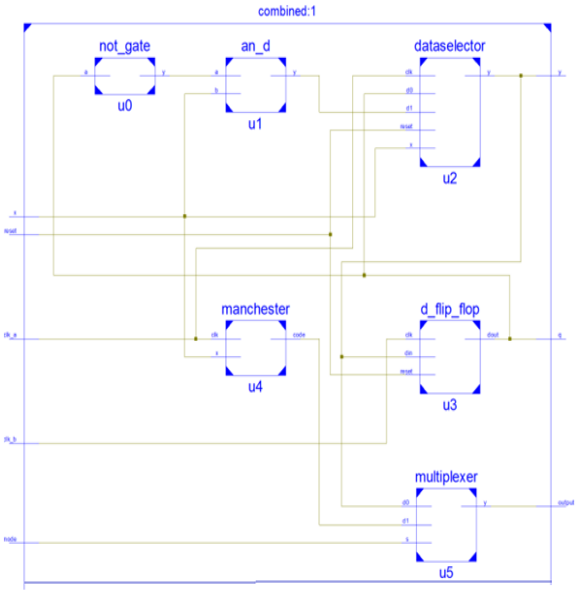

Fig.9.RTL of system

CONCLUSION

In this paper, the fully reused VLSI architecture for Manchester and Unipolar RZ code using sols technique is proposed. The similarity oriented logic simplification is divided in to area compact retiming and balance logic operation sharing. The first methodology reduces the number of components and the second methodology exploits the similar characteristics of line codes and allows effective hardware utilization of available components. We can say that it is achieved up to some extent. The coding diversity between Unipolar RZ and Manchester code seriously limits the potential to completely reuse the available hardware components to design a fully reused VLSI structure. The results show that the average use of components is improved and there is a reduction in the number of transistors. The number of transistors can be reduced further by developing an appropriate substitute for data selector.

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