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Implementation of an efficient ALU using Reversible Logic Gate

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***Abstract*— The paper proposes an idea of implementing an ALU circuit using reversible logic technique. Many reversible gates have been invented and they find useful applications in circuit design especially in the field of area reduction and power reduction. This paper uses MG Reversible gate and using this gate together with some conventional logic gates an ALU is designed performing logical, arithmetic, multiplication and shifting operations. The main aim of the project is to compare the proposed circuit with conventional ones in terms of transistor count, area and power consumption. The proposed system has been designed, programmed in VHDL language and verified using Xilinx ISE Design suit 14.2.**

***Index Terms*—ALU, MG gate, reversible.**

I. INTRODUCTION

Designing of a complex digital system which dissipates low power is a competitive topic in the research field of hardware design. Because complexity of the system gives rise to a problem of heat dissipation in the circuit and this becomes the critical limiting factor, we have to think more about how to resolve those challenges that mainly include area reduction in circuits. So, the complexity of the system will increase the energy dissipation or heat dissipation also increases with the exponential rate as the system hardware expands. So to reduce the complexity of the system hardware we have to mainly reduce the components in the system. As the number of components are reduced so ease to see a lower power consuming circuit. Here in this paper an efficient ALU circuit is implemented using a reversible logic gate together with some other conventional gate and the main idea behind the paper is to highlight the difference between an ALU that would have formed using already existing circuits and the newly proposed ALU. This has been represented in the paper that is an ALU which utilises less area when compared with existing circuit. Hence low power consumption and reduced circuit complexity able to be achieved.

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations.it represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPU contains very power and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU). Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers. A register is a small amount of storage available as part of a CPU. The control unit tell the ALU what operation to perform on that data and the ALU stores the result in an output register. The control unit moves the data between these registers, than ALU, and the memory. An ALU performs basic arithmetic and logic operations. Examples of arithmetic operations are additions, subtraction, multiplication and division .Examples of logic operations are comparisons of values such as NOT, AND and OR. All information in a computer is stored and manipulated in the form of binary numbers, i.e. 0 and 1.an ALU has a variety of input and output nets, which are the shared electrical connections used to convey digital signals between the ALU and external circuitry. When an ALU is operating, external circuits apply signals to the ALU inputs and in response the ALU produces and convey signals to external circuitry via its outputs.by using suitable conventional logic gates together with a novel reversible logic gate called MG gate an efficient low power ALU has been designed and simulated. Comparative results are presented in terms of number of gates and power consumption.

The MG gate is utilised in the implementation of a novel arithmetic logic unit. The ALU in addition to performing same logical calculations as MG is also able to perform arithmetic operation that is full adder and full subtractor, multiplier and a shifter. For this the circuit utilises conventional logic gates together with the proposed MG gate. The developed circuit has been compared in terms of gate count with excising ALU performing the above same operations. All existing ALUs make use of at least one MUX to implement the different processor operations one at a time. But the proposed circuit not only gives the results of all the operations together but also reduces the area needed for a MUX since MG gate itself is a MUX or in other words it's called as MUX gate.

II.EXISTING SYSTEMS

The existing systems give an idea of the already implemented circuit designs for performing various ALU operations in a system. The four main operations namely logical, arithmetic, multiplication and shifting operation have been represented with their currently implemented circuit designs. Hence this section will give an overall idea about the circuit width in terms of transistor count which in future will be useful to calculate area and power dissipation. First we will focus on the logic unit.it is one of the main unit in ALU to calculate the logical operations.

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A. Logical operation

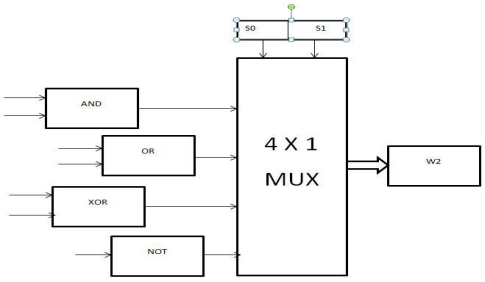

Fig.1 logic unit [1]

The above fig.1 shows the logic unit in ALU which is capable of performing 4 different logical operations AND, OR, XOR and NOT operations. Bitwise operation is performed on the two inputs. The operation to be performed is decided by two selections s1 and s0 as shown in the table table.1.So for this a 4 by 1 MUX is used to select one among the four logical operations. This already existing logical unit consumes in total 11 conventional logic gates. [1]

S1	S0	OPERATION
0	0	AND
0	1	OR
1	0	XOR
1	1	NOT

Table.1 logical operations [1]

B. Arithmetic operation

Arithmetic unit is yet another unit that constitutes the operations involving addition, and subtraction. The following figure fig.2 shows a circuit where both addition and subtraction operations are carried out in one single circuit.

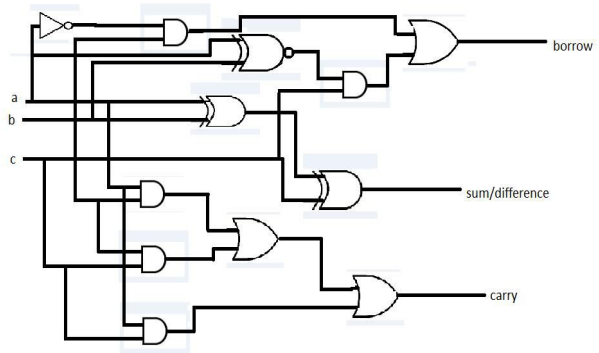

Fig.2 arithmetic operation

This is a conventional circuit where a, b are the inputs and the output is given by sum/difference, borrow and a carry bit to store the carry. The circuit indicates that it requires 12 conventional logic gates to implement the above operation.

C. Multiplier operation

Next is the multiplier unit involving in carrying out the multiplication operation. The figure fig.3 represents a simple circuit to carry out this operation. It is again an already exiting circuit indicating that it make use of in total 8 logic gates to carry out the result.

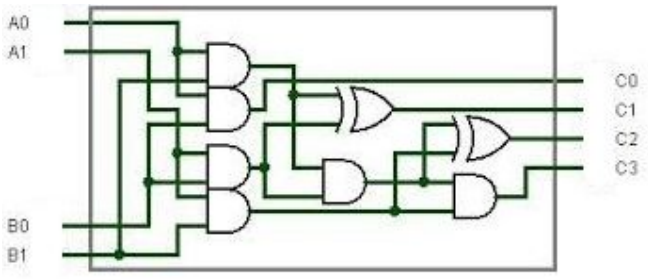

Fig.3 multiplier operation

D. Shifting operation

Shifting operation is also an important function to be installed in an efficient ALU. Hence the paper also considers his operation first by analysing the previous existing structure.

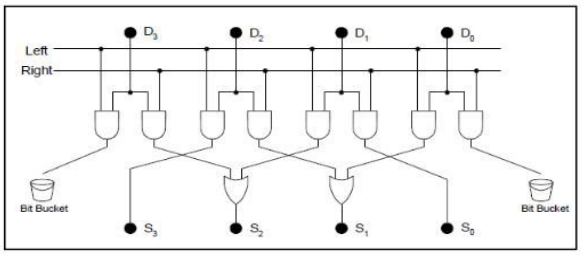

Fig.4 shifter unit

A logical shift is a bitwise operation that shifts all the bits of its operand. The two base variants are the logical left shift and the logical right shift. This circuit can shift the input bits left or right, depending on which control line is active. A shifter is a combinational circuit with one or more inputs and an equal number of outputs. The outputs are shifted with respect to the inputs. The above figure fig.4 discards any signal shifted out. However, the bit shifted out is of interest. In a right shift, it is the reminder afters division by two. In a left shift, it can be tested for significance so that the results of a left shift can be evaluated for validity. The bits shifted out are available from the AND gates at the extreme left and right of the circuit. The above existing shifter circuit implements logical shift operation performing both left shift and right shift according to the select lines l1,l2,l3,l4(for left shift) and r1,r,2,r3,r4 (for right shift).D0,D1,D2 and D3 are the four inputs and S0,S1S2 and S3 are the corresponding outputs from the circuit.it can be seen on expanding the circuit that it utilises 10 conventional logical gates in total to perform the logic shift operation. The circuit also contains two bit buckets to collect or store the extra bits that come from LSB or MSB upon the shift operation.

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III.SYSYTEM DESIGN

The proposed system makes use of a gate which is reversible in nature. The concept of reversibility is brought here and this gate namely, MG gate is the heart of the system. [2].A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Reversible logic is very useful for the construction of low power, low loss computational structures which are very much significant for the construction of arithmetic circuits used in quantum computation, nanotechnology and other low power digital circuits. . The most important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, HNG gate and MG gate. Here in this paper, only MG gate is utilized and analyzed.

Fig.5 MG Gate [2]

MG gate has 5 inputs i.e. A, B, C, D, and E and 5 outputs i.e. P, Q, R, S, and T. Output vectors have following expressions:

1) P = A,

2) Q = A XOR B,

3) R = (A XOR B) XOR C,

4) S = AB XOR D and

5) T = ((A XOR B) XOR E) XOR (AB XOR D)

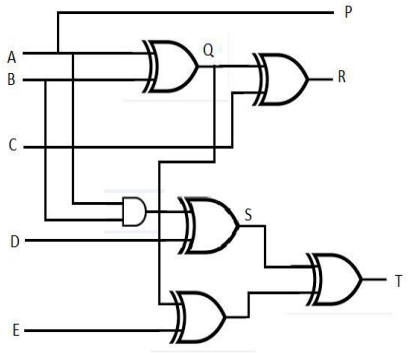

Fig.6 MG gate internal circuit diagram

The above figure 6 represents the internal circuit diagram of the used MG gate. The circuit has 5 inputs and 5 outputs; hence it is a 5 *5 reversible gate since the number of inputs equal to the number of outputs.

C	D	E	R	S	T
0	0	0	A XOR B	A AND B	A OR B
0	0	1	A XOR B	A AND B	A NOR B
0	1	0	A XOR B	A NAND B	A NOR B
0	1	1	A XOR B	A NAND B	A OR B
1	0	0	A NXOR B	A AND B	A OR B
1	0	1	A NXOR B	A AND B	A NOR B
1	1	0	A NXOR B	A NAND B	A NOR B
1	1	1	A NXOR B	A NAND B	A OR B

Table 2. Truth table of MG gate [2]

The above figure shows the proposed gate usually called as MUX gate and its corresponding truth table. A and B are the inputs and C, D and E are the select lines and Q, R, S, and T are the corresponding outputs. On expansion this gate
constitutes in total 6 conventional logic gates and implements6 logic operations. An additional NOT gate is added at input a to show the NOT operation. So in total 7 logic operations are involved. The cost of the MG is 7, and the worst-case delay is 7.

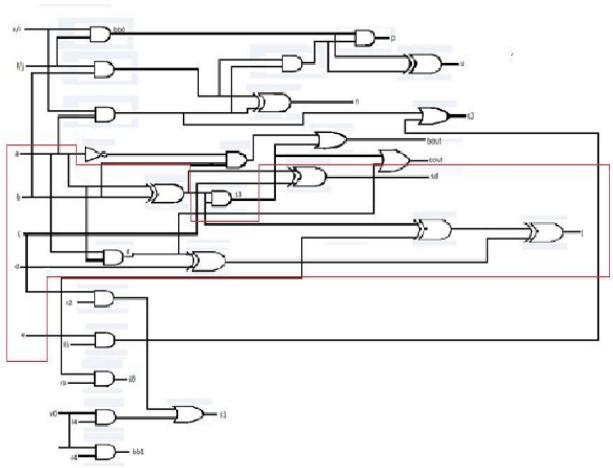

Fig.7 Proposed ALU

The above figure represents the internal circuit diagram of the proposed efficient ALU. The region enclosed in red line represents the proposed MG gate. The circuit utilizes 19 conventional logic gates including the proposed MG gate to implement the following four operations:

A. *Logical operation*

The MG gate is utilized. The 2 inputs to logic operation are “a” and “b” and the select lines are “c”, “d”, and “e” and the outputs are given in terms of “r”, “s”, “t” according to the truth table.

B. *Arithmetic operation*

Here “a”, “b”, and “c” are the three inputs and it computes both full adder and full subtractor in one circuit representing “sd” as the sum/difference, “br” as the borrow

and "carry".

C. Multiplier operation

It consists of "i", "b", "j" and "a" as the binary inputs and "g", "u", "n" and "p" are the outputs.

D. Shifting operation

Here both right shift and left shift operations are performed according to the select lines "l1", "l2", "l3" and "l4" (for left operation) and "r1", "r2", "r3" and "r4" (for right operation).The inputs are "v0", "x", "y" and "z" and outputs are "s0", "s1", "s2" and "s3".

VI.SIMULATION AND RESULTS

The following table shows the result comparison of the existing system with the proposed system in terms of the number of gates.

UNIT	EXISTING	PROPOSED
ARITHMETIC	12	4
LOGIC	11	7
MULTIPLICATION	8	7
SHIFTING	10	7
4 X 1 MUX	7	-
TOTAL	48	25

Table.3 Result comparison

A. MG Gate

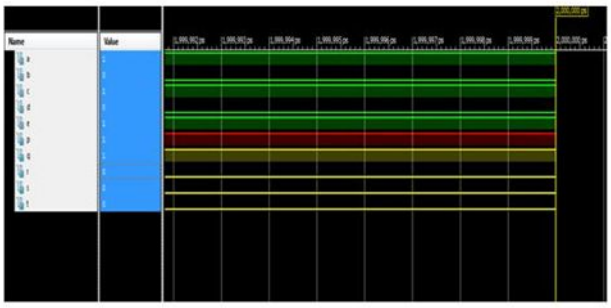

Fig.8 simulation result of MG gate

The graph of figure 10 shows the simulation result of the proposed circuit diagram in XILINX ISE design suite 14.2.From the graph we can see that "a", "b", "c", "d" and "e" are the inputs represented in green color and "p" is the output representing the input "a" recovering from it and is given in red color and "q", "r", "s" and "t" are the outputs given in yellow color representing the outputs of various logical operations.

B. Proposed ALU

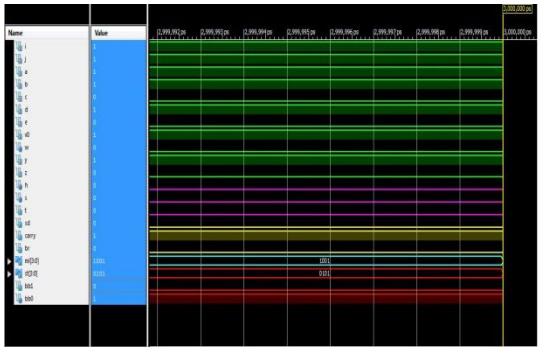

Fig.9 simulation result of proposed ALU

The graph above shows the simulation result of the proposed circuit diagram in XILINX ISE design suite 14.2.The different operating units are given different signal colors in the result. Green color indicates the input lines. Pink lines show the output of logic operation. Yellow lines show the output of arithmetic operation. Blue line indicates those of multiplication operation and red region represents the shifting result.

As mentioned earlier the fig.9 depicts that all the 4 ALU operations have been carried out at the same time and there is no need of a multiplexer unit to select a particular operation. Hence the space and power consumed by a multiplexer can be eliminated.

V.RTL SCHEMATIC

The following figures 12 and 13 shows the RTL schematic of the utilized reversible MG gate and the implemented ALU, respectively in XILINX ISE design suite 14.2.

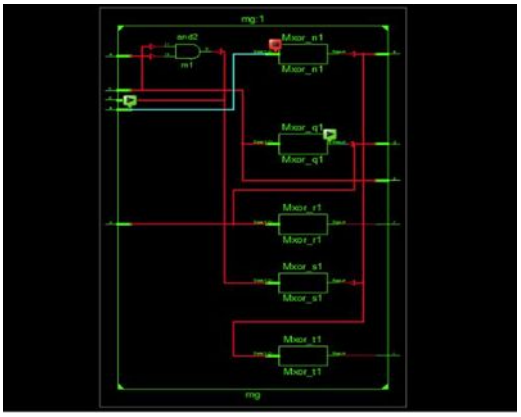

Fig.10 RTL schematic of MG gate

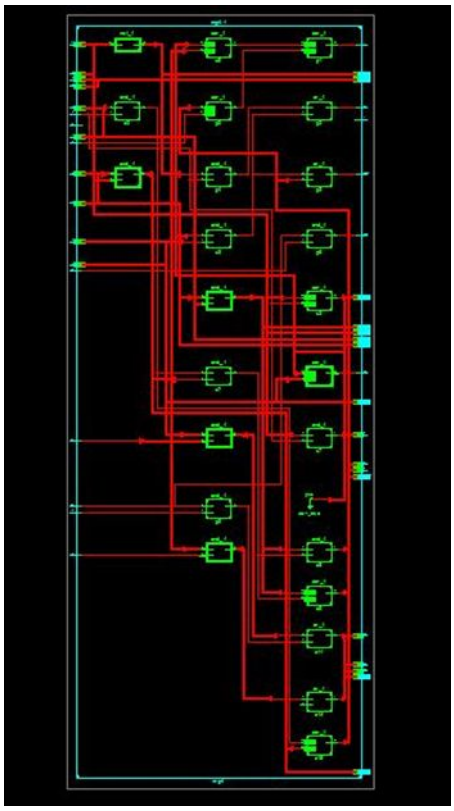

Fig.11 RTL schematic of proposed ALU

VI.DESIGN SUMMARY

The following figures 14 and 15 shows the design summary of the implemented proposed ALU in XILINX ISE design suite 14.2.

Fig.12 Design summary of MG gate

The Design Summary in Xilinx allows us to quickly access the design overview information, reports, and messages. By default, the Design Summary appears in the Workspace when one opens a project, and it displays information specific to theirs targeted device and software tools. The panes on the left side of the Design Summary allow us to control the information displayed in the right pane.

Fig.13 Design summary of proposed ALU

The fig.13 shows the number of LUTs used and the utilization percentage of IOBs and some other relevant information. The utilization percentage is 26%.

VII.CONCLUSION

A novel 5*5 programmable MG gate was proposed and verified that may calculate of AND, NAND, OR, NOR, XOR, XNOR and NOT depending on the inputs from the programmer. The proposed MG gate has been implemented in the design of a novel quantum arithmetic logic unit, and its design has been compared with the existing work in programmable ALU design. The novel ALU required only minimal increase in quantum cost and delay due to the MG design, which also allowed for increased functionality for the computing machine there by doing multiplication, arithmetic and shifting operation together with the logic function. An ALU is a major component of a computing device and is the core component of central processing unit. Moreover, it is the heart of the instruction execution portion of every computer. An ALU is a multifunctional circuit that conditionally performs one of several possible functions on two operands A and B depending on the combinations of selection inputs. The low power dissipation of proposed ALU makes it more useful in less power requirement applications.

VIII. FUTURE SCOPE

The above ALU reduces the gate count and thus saving more area and reduced power consumption. As a result the circuit can be more extended to higher number of bits and increased number of operations. Also lot of other reversible logic gates is available and hence they can be combined with the above MG gate and implement more enhanced ALU operations. Moreover ALU can be used in applications such as quantum computing, nanotechnology, optical computing, low power VLSI designs, etc. The extended operations will be more useful for doing complex logic designs. Many ASIC"s based projects could be possible by using the proposed ALU design.

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