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An advanced Reconfigurable architecture for implementing FIR filters using DA technique

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***Abstract*— In signal processing, the function of a filter is to take away unwanted elements of the signal, such as random noise, or to extract useful elements of the signal, such as the components lying at intervals a particular frequency vary. FIR filter are inherently pipelined. DA- based design use lookup tables (LUTs) to store recomputed results to scale back the computational complexness. This paper presents the realization of FIR filter of large order for reconfigurable architecture using distributed arithmetic (DA) based techniques. This proposed structure involves significantly low complexity design, significant saving of computation and memory.**

***Index Terms*— Block processing, finite impulse response (FIR) Filter, DA formulation, reconfigurable architecture**

I. INTRODUCTION

Filters are electronic circuits that perform signal process functions, specifically to remove unwanted frequency parts from the signal, to enhance wanted ones, or both. A filter is an electrical network that alters the amplitude and/or section characteristics of a signal with reference to frequency.

Ideally, a filter will not add new frequencies to the sign, nor will it amendment the part frequencies of that signal, but it can amendment the relative amplitudes of the varied frequency parts and/or their section relationships. Filters are usually used in electronic systems to emphasizes signals in bound frequency ranges and reject signals in alternative frequency ranges. Filters are wide utilized in signal process, digital communication systems like channel equalization, noise reduction, radar, audio and video signal processing, biomedical signal handling, VLSI.

There are two sorts of filter: analog and digital. FIR Filter is the one of the type of digital filter, which can be used to perform all types of filtering. A filter is a device that passes electric signals at definite frequencies or frequency ranges whereas preventing the passage of others. Filters are wide used in signal processing and digital communication systems like channel equalization, noise reduction, radar, audio and video signal processing, biomedical signal handling, VLSI.

Reconfigurable finite-impulse response (FIR) filter whose filter coefficients dynamically change throughout runtime plays associate vital role within the various systems such as software defined radio systems.

Finite impulse response (FIR) digital filter is used in many digital signal processing system, such as speech processing system, loud speaker equalization system, echo cancellation system, nose cancellation system, and various communication system. Many of these systems need FIR filters of huge order to fulfill the rigorous frequency specifications. Very usually these filters have to be compelled to support high sampling rate for high-speed data communication.

II. METHODOLOGY

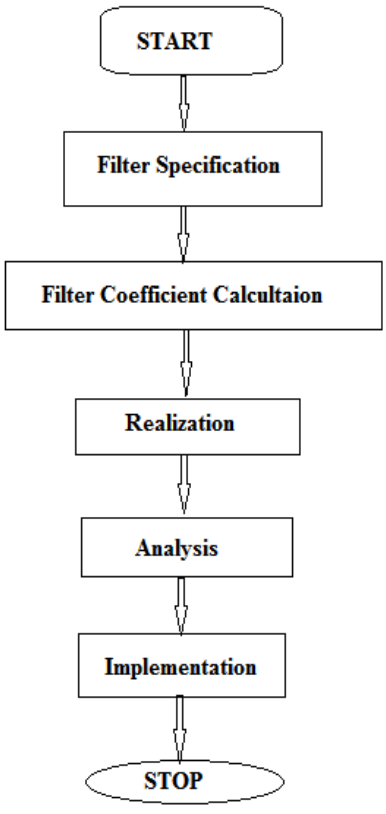

Fig 1- Flow Diagram

The design of a digital filter involves following 5 steps.

[1] Filter specification: This may embrace stating the sort of filter, for example the desired amplitude and/or phase responses, low pass filter, and also the tolerances, the sampling frequency, the word length of the input data.

[2] Filter coefficient calculation: In filter coefficient calculation the transfer function H(z) coefficient is determined in such a way that, it can satisfy the given specification. The choice of coefficient calculation technique are going to be influenced by many factors. The most important of that are the important necessities i.e. specification. The window, optimal and frequency sampling technique are the most ordinarily used.

[3] Realization: The realization of FIR and converting the transfer function into a appropriate filter network.

[4] Analysis of finite word length impacts: The effect of quantizing the filter coefficients and data input and the effect of the filtering Start Performance specification, calculation of filter coefficients Realization structuring the world length effects analysis the H/W or S/W implementation Stop operation using fixed word length on the filter performance is analysed here.

[5] Implementation: Implementation involves producing the software code and/or hardware and checking the performing of the actual filtering.

III. BLOCK DIAGRAM

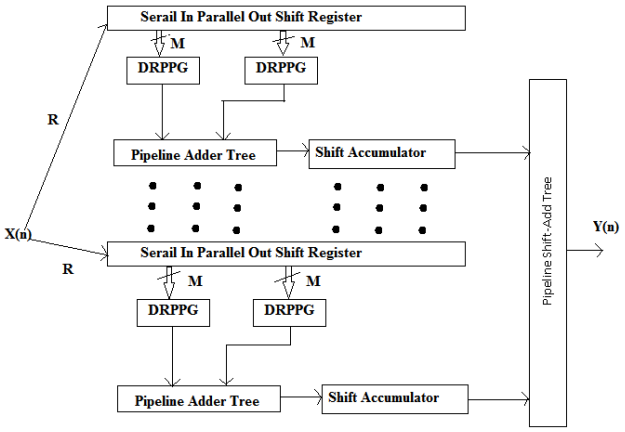

Fig 2- For FPGA implementation, structure of DA-based FIR filter. (a) DA-based FIR filter ,DRPPG for M = 2 and R = 2.

A distributed arithmetic (DA) technique has increased day by day in recent years for its high- output process capability and redoubled regularity, which result in cost- effective structure. The main operations required for DA- based technique are mostly computation and a sequence of lookup- table (LUT) accesses which are followed by shift accumulation operations of the LUT output.

The DA-based structure used for the implementation of an FIR filter assumes that impulse response coefficients are fixed and it possible to use ROM-based LUT. The memory requirement exponentially increases as the order of the filter increases for DA technique based implementation of FIR filter. To eliminate such problem of large memory requirement, we need to use rewritable random access memory (RAM) based lookup table (LUT) instead of read only memory (ROM) based LUT. The structure of the proposed DA method based FIR filters using DRAM.

To implement, the proposed structure has q sections, and each section consisting of P DRAM-based RRPGs (DRPPGs) and therefore the PAT to calculate the addition, followed by shift-accumulator that will perform over R cycles according to the second addition. However, we will use dual-port DRAM to scale back the whole size of LUTs by 0.5 since 2 DRPPGs from 2 totally different sections will share the only DRAM. The proposed structure will turn out QP partial inner product in a single cycle, whereas the can generate lp inner product. In the rth cycle, the qth sections generate P partial inner products and it will be added by the PAT and the outputs of the PAT are accumulated by a shift-accumulator over R cycles.

Finally, the PSAT produces the filter output using the output from every section each R cycles. The accumulated value is reset each R cycles by the control signal [acc_rst] to keep the accumulator register able to be used for calculation of the next filter output. The proposed structure will support the input sample rate of fclk/R, if the maximum operating clock period is fclk.

IV. RESULT

TABLE- I
Performance comparison

Design	Number of slice Flip Flops	Number of LUTs	NOS
Structure of [1]	-	517	205
Proposed structure R=2	79	52	56

The proposed DA structure is written in hardware description language and synthesized by design compiler. From the synthesis result it is found that the proposed design occupies the smallest silicon area when M=2, therefore the value of M is set to 2. The proposed structure has the less area.

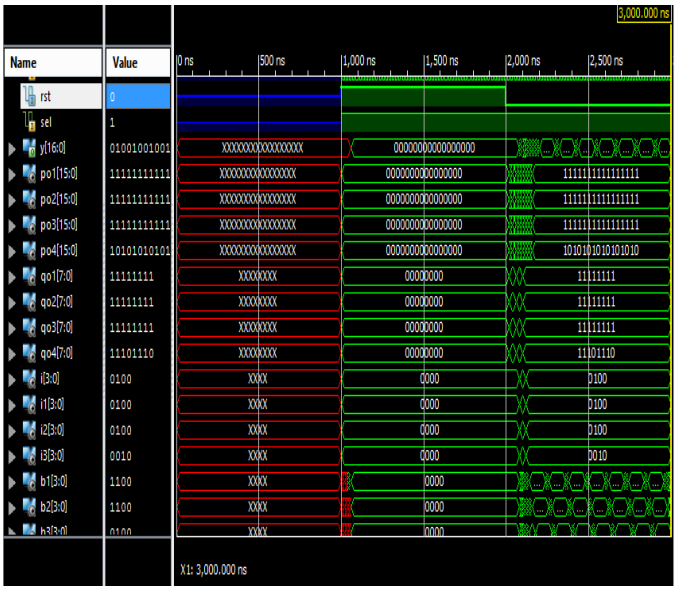

Fig 3- Simulation Result

V. CONCLUSION

It is shown that the hardware cost could be reduced by sharing the same registers by the DA units for different bit slices. It is found to offer less number of slices than the earlier structure. This paper presents the realization of FIR filter of large order for reconfigurable architecture using distributed arithmetic (DA) based techniques. This proposed structure involves significantly low complexity design, significant saving of computation and memory.

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