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HIGH SPEED BANDWIDTH MANAGEMENT FOR SERIAL DATA TRANSMISSION

BHAGYALAXMI, DR.BASWARAJ GADGAY, SUMAN B. PUJARI

Abstract- **In order to elucidate many problems surfacing when applying the ideas to bandwidth management and latency in a large industrial multicore system-on-chip (SOC) is most important matter of interest, so it can be resolved by many techniques. Along with that significant challenge is associated with scheme, flow, and tools which are posed by these delineations. For the realistic applications, the solutions rendered here will hold good for efficient handling of many physical constraints of the system.**

In any distributed and for any control systems, even fixed-latency in any serial lines is considered as most important parameter. When consistently power-up or reset the transceiver, even the most high-speed, highly efficient Serializer-Deserializer (SerDes) chips do not keep equivalent link latency throughout its data transmission along the length of its link. Hence to overcome this, we had effectuated here few techniques to have a fixed-latency of transceiver.

Index Terms- Bandwidth, PISO, SerDes, SIPO, Transducer.

I. INTRODUCTION

In today's close surveillance one can easily ascertain that there is a large phenomenal breakthrough had taken place in the field of VLSI in terms of cut down in its area, power consumption, and its working cunctation. This had led to very much faster in there working and less ravenous towards power when it is being compared with respect to their progenitor, hence as a result they had grown very much quickly and its demand had increased drastically. Hence they had property to work along different types of IPs which are accomplished to toil with alternate clocks which works at number of voltages stratums [1]. In the view of any person, communication is nothing but it's just connoting to put across intended information upon some correlative understandable cipher with or without usage of channel.

Any two devices which need to communicate have to follow only two types of communications: I) parallel type and II) serial type. The main motto of these types is to convey the data without loss in its statistics. In first type shown in fig. 1, the information will be in large content which will be transferred to the other end of the transmission simultaneously.

At the same time the other type shown in fig. 2, will also have large amount of content but it will be transferred bitwise that is nothing but sending one bit after the other hence the cost will be decreased to maximum extend. The name serial will not only define that it is a sequential data transfer but they were organized for the broadcast which has to be well ordered as well as unimpeachable. But basic difference which will differentiate both of them is by using the conductors which were present at their different layers of communication.

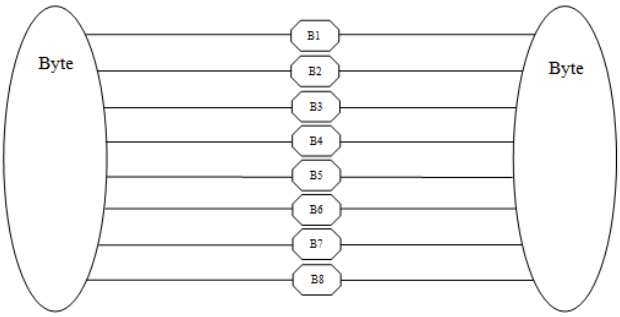

Fig. 1 Diagram of Parallel Transfer

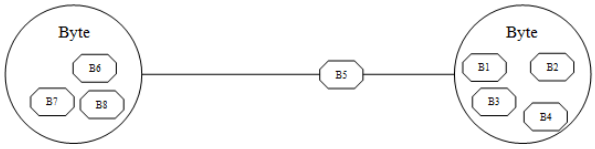

Fig. 2 Diagram of Serial Transfer

Although there exists lots of merits along with first type, since the parallel data transmission will be asserted with unvarying clock signals which uses disarticulate lines in the parallel line cable; hence such type of transmission is known as synchronous and when compared with first type, few merits were associated with respect to second type in terms of skew of the clock, complexity, crosstalk etc.

It can be asynchronous in nature or synchronous in nature as well. Hence serial type of communication will plays very much crucial role in our modern system of communication which was directly affecting the cost, performance of the overall system.

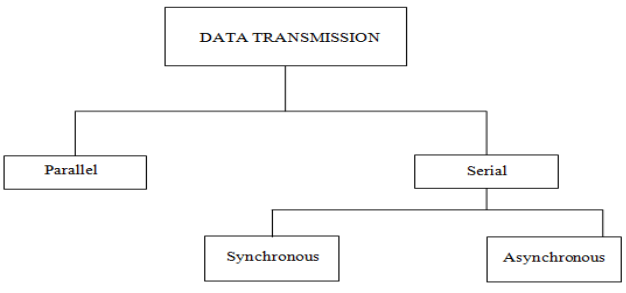

Fig. 3 Nomenclature of transmission of information

One of the most popular devices which will follow this type of serial communication is SerDes (serializer and deserializer); though they work at higher rates but there latency will not keep constant over the paths of channel after every turning on and off, or resetting activities. Hence it had become desirable to achieve almost fixed and constant latency of the transceivers like TKL2711, SCAN25 100 etc, [1, 2]. The very first experimented transceiver is GBT (gigabit) and another one was achieved by the CERN, which was having the precision up to the length of around 10 to 12 km.

The basic function of any serdes is used for the transmission of information which will be in the form of parallel transmuted as that bit streams in the form of serial and once it was transmitted the data will be in the form serial streams of bits will be retrieved as parallel streams of bits.MGT (multigigabit) is one among of such types of serdes, and also have one unique property whose line rate will be almost equal to the one gigabits per second or above; due to this property they will be known as 'DATA HIGHWAYS'.

II. LITERATURE SURVEY

[1] The research association known CERN was mainly focused on the controlling, triggering and timing signals which must be equally shared to many large numbers of electronic devices or systems within the propinquity of many triggering central processors from a very single orientation. Here the author focused on many highly powered laser sources which can be considered as atop to an optical fibre networks which were used for broadcasting different signals to various culminations with the help of optical multiple channel distribution systems. Some systems had got capability to prototype the several methods to multiplex the decision of level trigger with the commands of broadband and that are transferred through the optical lines through laser which were relatively very good at speed.

Because of these ideas the advantage associated with this paper is as follows: few numbers of sources which are known as laser sources were installed in the set-up due to which it will be feasible for optimization of system performance, tenability because of some feedback controllers which were providing some meticulous value of temperature,. It allows for the synchronous transmission of broadband orders or commands at a given interval of time, parameters or commands which are addressed independently such as masks, data which are calibrated can also be provided.

CERN worked hard in order to get easiest methods henceforth he had brought up many techniques for the conveyance of very large phase references RF signals using optical fibres lines. Even though working so hard he had faced many problems and many disadvantages are associated with this paper and one is clock which was used as a reference was having the jitter which increased while sending through the transmitter which in turn increased the level of attenuation.

[2] Here in this paper the authors V. Izzo et. al[2]., was conceived an idea of reinforcing the new architectures which can lead to the high performance transceivers. These ideas can be submerged to get newest and fast working generations of transceivers. The systems will use two different types of configurations. Whenever a power cycle will get completed there exists no loss of data during its transmission hence this type of transmission is referred as synced pipelined transmission.

Such designed systems can have ability to withstand large changes in its latency value since they won't depend on encoding which was done serially. Hence the author had strived to develop such valid designs which can have at least non-fluctuation latency transceivers which in turn we can achieve low power dissipation, cost required for its construction will be very much low and integration of whole system will be of great accuracy. Nevertheless such attempts had been performed in this paper but it was not that successful hence it had been considered here as a future work.

Here the author was mainly emphasized on the one which was also most compatible with apparatus such as LHC toroidal since they are synchronous and provided with well architecture. There exists customized board which are known as crates such as VME, which had the capability to enhance the working of receiver parts due to which the efficiency of system was got increased. Some outputs which were termed as "x1, x2, x3....." are considered for phase compensating, since large number of buffers where used which were ensuing the delay. Hence to overcome such complication the DLL with 2x outputs were used.

The main advantages achieved was that it is less deployed by serial route due to this the value of different parameters will remained almost unchanged till the completion of transmission since such configuration was developed such that it will reset automatically for every 3 to 4 seconds and will keep the track of changes in the values of its latency.

[3] The paper mainly focuses on the author's experiments in order to get the authentic system known as Compressed Baryonic Matter (CBM). This experiment was broadly used in data acquisition (DAQ) mechanism. The forte of this CBM system is that it can rely on a single fibrous link for any number of networks which were used in applications having a single bidirectional network system and hence it will be helpful in developing new protocols. According to the experiments performed, results obtained by the author was that the networks using CBM will have to use some protocols which were accounted into different functions and at the same time they need to access same fibrous links which will subdue length curtailment.

The main objective of this paper was to get beam of higher intensities, highest energy and highest power so that they can be used in application of parallel usage, along with that some tolerance ability of front and back end part had to be augmented. Owning to this many advantages where related to this paper since lot of protocols that are developed can be re-transmittable because of different types

of traffic classes. When these classes are inserted into the networks then packets of information are sent with negligible amount of latency. The information will be previously stored in the re-transmittable buffers of transmitter and if exact data will be reached to receiver part and if it sends back the positive retort then buffer will be freed else once again information has to be transmitted through the same line.

Major disadvantages associated with this paper are as follows: since many protocols which were generated will be characterized with the attribute to find out where the errors are occurring that to single or double bit errors but when errors will occur then it results into multiplication of errors in the code word which is of 8 bits, hence to perceive these errors costs will be very much high and hence results aloft in bandwidth.

III. PROPOSED METHOD

As VLSI not only deals with the ics, but it is also tutelage of many signals being in use. Among them signals like I/O will have lots of recital in the system's proper working, so lots of factors for the exact and appropriate concentration has to be provided to the quality of the systems being used for the particular provision.

In some of the industrial applications and also in some of the system company's which is solely depended on the computer will have I/O s which is very essential role to play. As now sophistication had reached to high level, reliability of the I/O communication had problem that is initially aroused to higher. Traditionally, there are many alignment problems to the parallel I/O bus. As the speed is high for the digital devices proportionally delays associated along signals cause problem.

In order to have solutions for above problems as they are the pioneer of solution design engineers had hosted many acceptable methods to have greater speed and less I/O inconvenience caused by them.

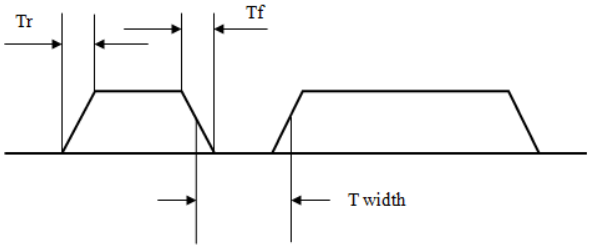

Fig. 4 Digital Signal which is standardized

The fig. 4 is all about digital signal which is used by any GBT.Let few values of rise time width is being calculated along with fall time are noted below. Tr = 40picosec, Tf = 40 picosec, T width = 0.20nanosec. The fig. 5 now drawn below is historical signal which is a reference that shows how much good and faster is above signal in fig. 4.

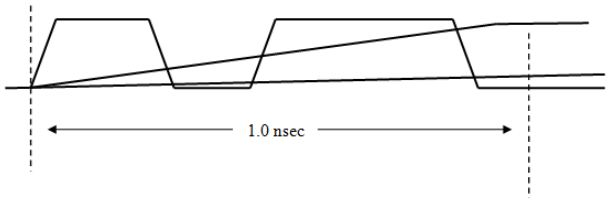

Fig. 5 Historical Digital signals

3.1 TIMING MODELS

Ics can have 3 basic models used to achieve the communication to occur with different other Ics and they are

- SYSTEM SYNCHRONOUS

This model was shown in fig. 6 was most traditional and yet effective since many years. Communication exists between Ics and only one standard clock was enforced to both Ics and also manipulated for transmitting and to receive. The model is shown in fig. 6 below. Accordingly all the data lines have to get connected to this standard clock which makes the designing part becomes strenuous.

- SOURCE SYNCHRONOUS

Time available was always such a large in recent years the delay always seems to be negligible in front of them. Many advances had happened increasing the speed alongside the delay seems to be very much larger and became difficult to manage. As such problems were overcome through sending a photocopy of the original clock all along the data. And this method is known as clock forwarded (i.e. source synchronous).

In this type models in fig. 7, the transmitting integrated circuit is designed to generate clock signal that holds the data and integrated circuits that one which will helps to receive the data will be using generated signal of clock for its reception.

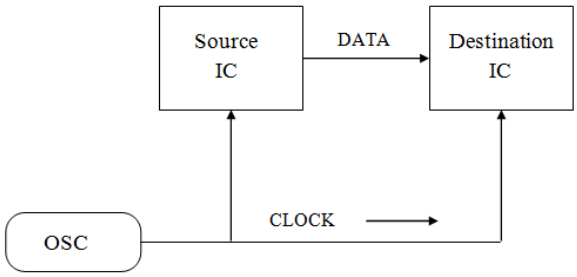

Fig. 6 Diagram for System Synchronous

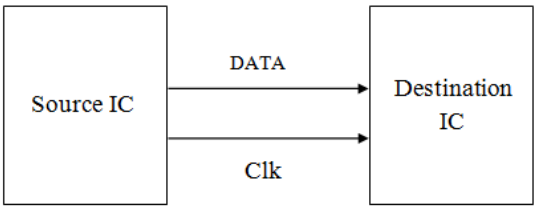

Fig. 7 Diagram for Clock Forwarded

- SELF SYNCHRONOUS

For any modern communication systems the main idea to have the less hardware implementation similarly the same idea was executed in this type of application model. For any communication holding two different Ics, then one is for transmission the data and the other will be for the receiving application.

The one which is being used for the transmission of the data along with which the clock was embedded i.e. both data and clock is contained. The model was in fig. 8 shows self synchronous.

The model with that idea is used in project so that hardware can be reduced. The main implied today's systems are in conversion from parallel and to directly to get serial, in SER-DES, also in serial conversion to that of parallel. These will all have merits and along with they had few demerits as well.

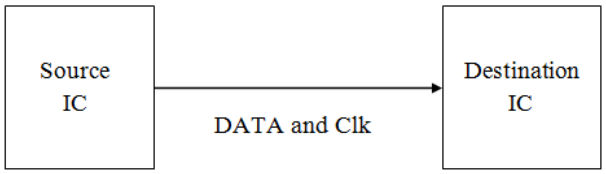

Fig. 8 Diagram for Self synchronous

3.2 PROPOSED BLOCK

The main solution to have bandwidth and latency of invariable values can be achieve through maintaining phase and clock is being provided along the data and is tried to maintain almost constant. The below fig. 9 is RTL view of system named as MAC.

RTL view will usually hide the overall system in built and upon checking out whole setup can be viewed. It has the inputs intermediate signals and outputs details. The next fig. 10 shows whole components and its connection with one another.

The following have transmitter part, decoder and respective receiver part which are being fanned with their different clock signals which are the merit and main reason to achieve good bandwidth and help to have less latency.

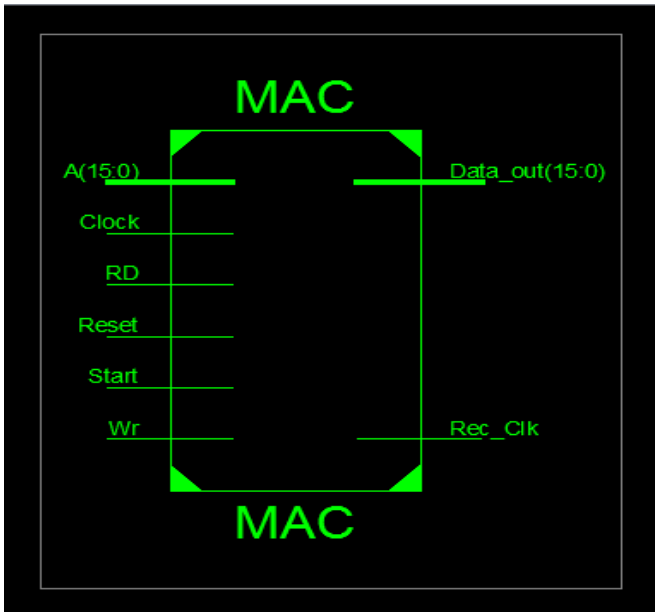

Fig. 9 RTL view schematic

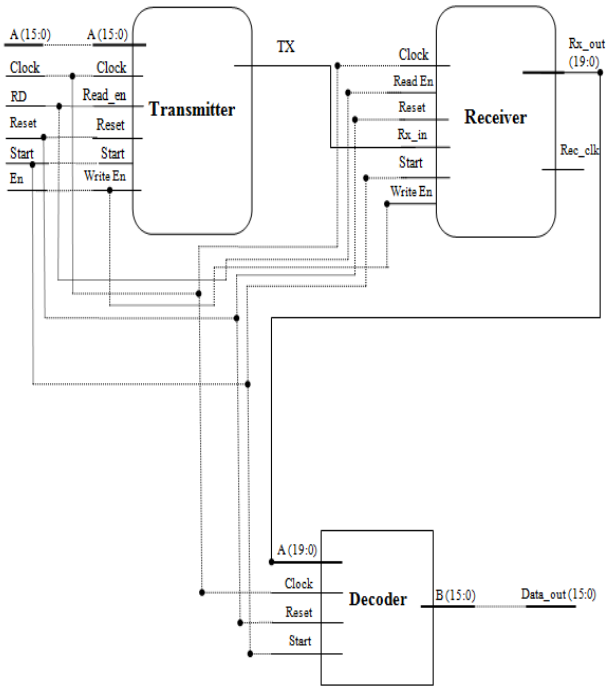

Fig. 10 Complete Block Representation

As now we are familiar that different clocks are provided to transmitter and receiver due to which one is belonging to user side and other to reception side. The transmitter part if we enlarge and analyse we get know that it is again made out of few components such as encoder, FIFO, PISO. Similarly in case of receiver there it is consists of SIPO, clockdiv blocks. The following shows the RTL view and its block diagrams. There is application of buffer (elastic) and FIFO to adjust phase to required level.

3.3 TRANSCEIVER TRANSMITTER PART

The followed fig. 11 and 12 will give whole proposal about the transmitter section of the transceiver.

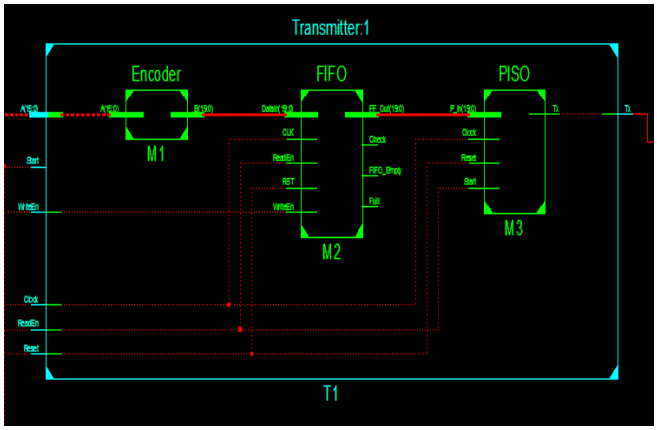

Fig. 11 RTL view (Transmitter Section)

The transmitter is made of three subsections as shown above, they are encoder (8bit and 10bit), FIFO and PISO. As it can be observed that they had placed in two sublayers one is PMA (physical medium attachment) and PCS (physical coding sublayer) and not only transmitter is placed even receiver will be placed in these sub layers.

In case of transmitter the layer PMA holds PISO and the layer PCS consists of FIFO, ENCODER. Similarly the receiver will have CDR, SIPO in the layer of PMA and clockdiv blocks in case of PCS layer [5]. Since PMA hold PISO helps to get serial output and parallel input, PCS will help to process data prior to serialization and later than deserialization.

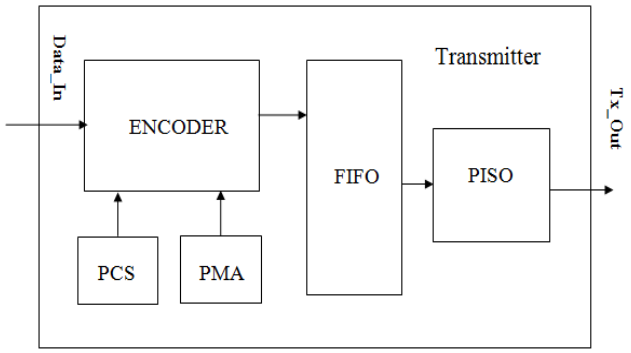

Fig. 12 Transmitter Section

3.3.1 DESIGN OF ENCODER

Initial value fed as input is of 16 bits parallel bit streams, which will get encoded to 20bits through 16bit/20bit encoder which is used for in this project. This scheme was extracted from 8bit and 10bit encoder developed and adapted by the IBM. It is the looked up scheme encoding where the bits of 8 is encoded to 10bits whose main reason they indirectly helps to better recovery of clock which in turn helps to get correct data at the other end of transmission. Before understanding the encoder working lets deem about the fiber channel levels.

The fig. 13 shows different levels of channel which was named as FC level 0, 1, and 2. The following shows it corresponding nature of working that is followed below.

1. At level FC 0, it consists of optical and physical interfaces, about cables used for various connections and different connectors as well for the connection purpose.
2. In case of level FC 1, the required 8 and 10 bit ordered set for the encode and decode function.

- Since ordered set are the different kinds of words used for transmission as well as for controlling function.
- These ordered set are made from four characters.
- But special characters are also utilised such as 10bits and also 8bits space.
- For example any data that is being encoded after encoding them one byte at a time when dealing with an 8bit byte then largest 8bit combination will be 0 to 255.
- If we got 10 bits, then we get 1024 combinations. It means 10bits combinations can be helpful in application.
- It has three important functions such as encode/decode, unique signalling and functions like controlling and link protocol for initial and resetting the link.
    - Now analysing level FC 2 it focuses on the exchanges, sequences, flow of the controlling and classes for services.

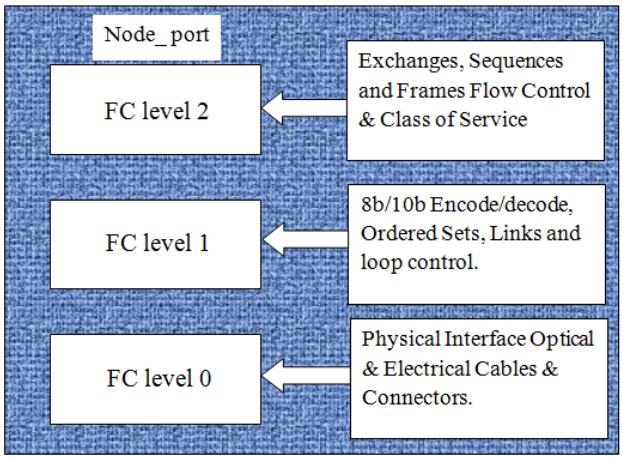

Fig. 13 Levels of Fiber Channel

3.3.2 PISO

The above shows RTL view of PISO which helps to get serial data out by converting it from parallel input. It is one of the main parts of the project. It is PMA which holds piso in its environment. It can be implemented using two different types.

One is using load shift register and it fig is shown below. The number of Dff (flip flops) is always equivalent to the num of input and their outputs is fed to the next ff as input where each clk positive edge one i/p bit will get

shifted and is taken as o/p which are serial in nature are stored in the buffer.

Other type is through revolving sector implementation and comparable to above its simple method. It consists normally counter, counts the parallel input and is fed to an ff and those will be held in buffer. Finally this one is being used here due to which output from this PISO is directed towards receiver.

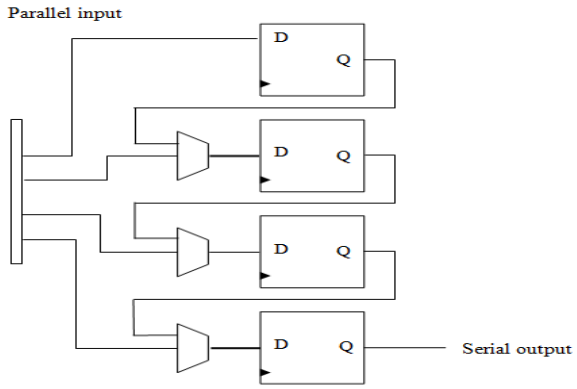

Fig. 14 PISO realization

3.4 TRANSCEIVER RECEIVER PART

The followed fig. 15 and 16 will give whole proposal about the receiver section of the transceiver. It is consists of SIPO, clockdiv, buffers, decoder. Compared to transmitter the receiver will have clockdiv blocks in case of PCS layer and at the same time Clock and data slider, SIPO in the layer of PMA [8]. The data which was taken from the transmitted side is taken through receiver with the help of SIPO.

The data which was fetch from the SIPO will be given to buffer which operates as FIFO. But here data from the sipo will be fed to clockdiv which is known as clock and data slider block. It will comprise of CDDA (i.e. comma detector and data alignment), DCPS (i.e. dynamic clock phase shifting), and CDT (i.e. changeable delay tuning).

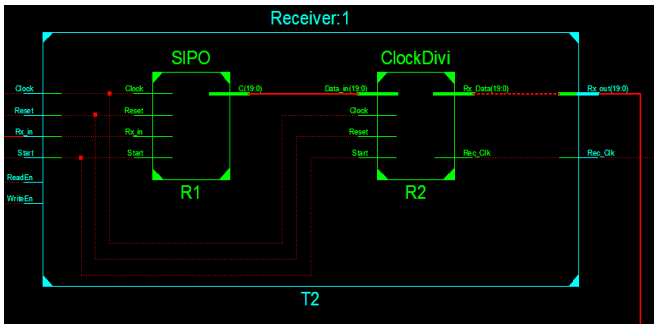

Fig. 15 RTL view (Receiver Section)

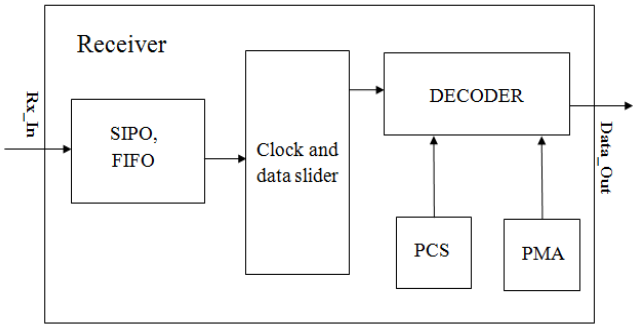

Fig. 16 Receiver Section

3.4.1 CDS (CLOCK AND DATA SLIDER)

The CDS is most important part of whole project which will helpful in retrieving data at the receiving end. The fig. 17 is the schematic of CDS which is comprised of three more components that are CDDA (comma detector and data alignment), CDT (changeable delay tuning) and finally DCPS (dynamic clock phase shifting).

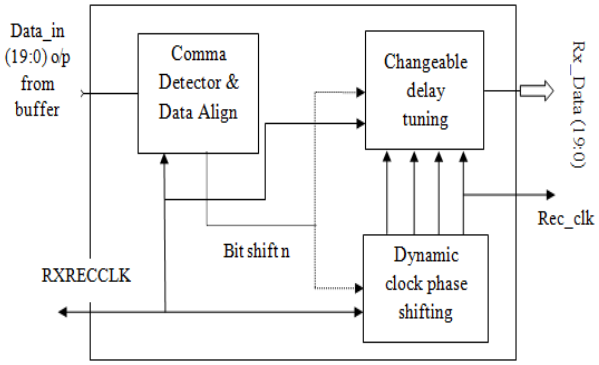

Fig.17 Schematic of CDS

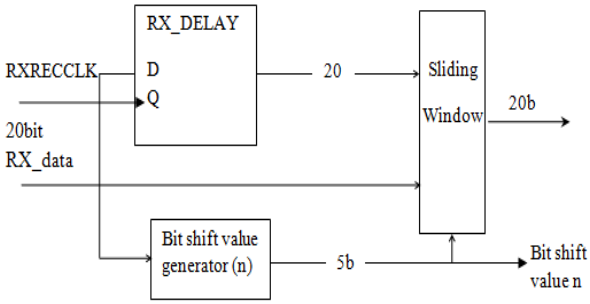

Fig. 18 Block Diagram of CDDA

IV. SIMULATION RESULTS

The above is the simulation result for the transmitter as shown in the fig. 19 Now START bit is high,

reset will be high initially but later on it has to set to zero, clock has to turn on, then

- The input data is given as 1100110011001100 which is of 16bits initially.
- As soon as Write_en will be high and Read_en will be low, then FIFO will write the content or output of encoder.
- If Write_en will be low and Read_en will be high, then FIFO will read the data which is stored.
- Since it consists of PISO will convert the parallel o/p that of FIFO to the serial bits and now this transmitter data will be given to the receiver.

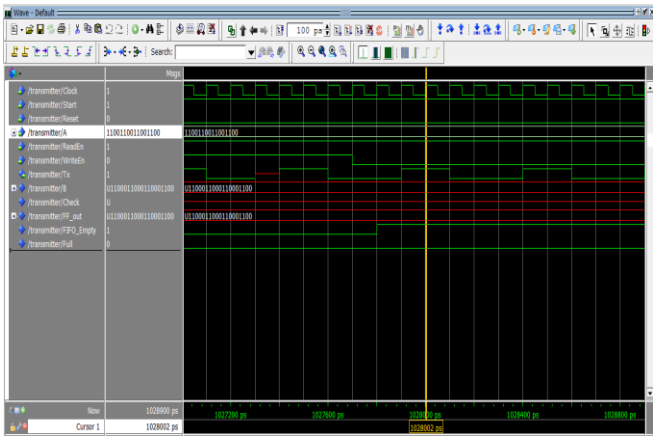

Fig. 19 Result showing for transmitter

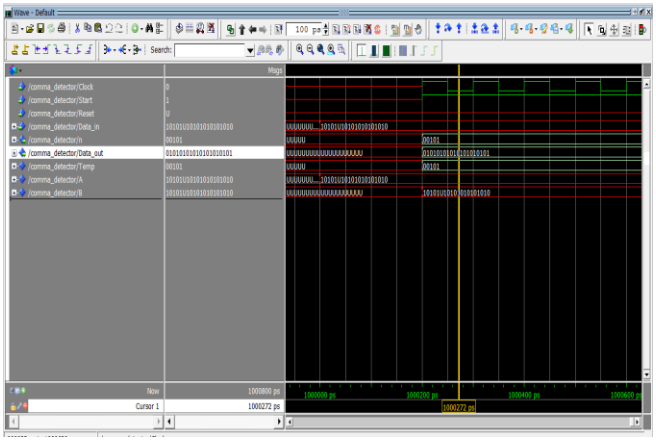

Fig. 20 Result showing for block of CDDA

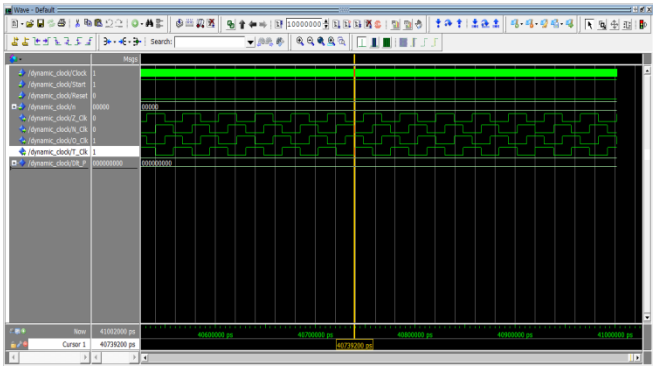

Fig. 21 Result showing for block of DCPS

V. CONCLUSION

Since today most of the transceiver which are being use in day today's application will always get changes in its latency values after every and each start up and turn off or even during reset operation. This is the main reason why the transceiver had seen less popularity in the world of communication.

Due to this few of the drawbacks whose solutions are obtained from the above project and had overcome the problems aroused during the existing mechanism. The requirement of reducing offsets of clock was done here which was drawback of pervious works and had almost achieved to have bandwidth & latency of some fix value and now tried that it will not get changed even after on, reset or off states.

The factors such as temperature, dispersion, pressure, jitter, humidity etc, were not considered here during the operations. Hence they had a large impact on the performance of the system. Hence the effect and impact of these environmental factors on transceiver working will be considered as theme of future work.

REFERENCES

[1] "B. G. Taylor, "TTC Distribution for LHC Detectors," IEEE Trans. Nucl. Sci., vol. 45, no. 3, pp. 821-828, Jun. 1998".
[2] A. Aloisio, F. Cevenini, R. Giordano, and V. Izzo, "High-speed, fixed-latency serial links with FPGAs for synchronous transfers," IEEE Trans. Nucl. Sci., vol. 56, no. 5, pp. 2864-2873, Oct. 2009.
[3] "F. Lemke, D. Slogsnat, N. Burkhardt, and U. Bruening, "A Unified DAQ Interconnection network with precise time synchronization," IEEE Trans. Nucl. Sci., vol. 57, no. 2, pp. 412-418, Apr. 2010".
[4] A. Aloisio, F. Cevenini, R. Giordano, and V. Izzo, " Emulating the GLink chip set with FPGA serial transceivers in the ATLAS level-1 Muon trigger," IEEE Trans. Nucl. Sci., vol. 57, no. 2, pp. 467-471, Apr. 2010.
[5] "R. J. Aliaga, J. M. Monzo, M. Spaggiari, N. Ferrando, R. Gadea, and R. J. Colom, " PET system synchronization and timing resolution using high-speed data links," IEEE Trans. Nucl. Sci., vol. 58, no. 4, pp. 1596-1605, Aug. 2011".
[6] R. Giordano and A. Aloisio, "Fixed-latency, Multi-Gigabit serial links with Xilinx FPGAs," IEEE Trans. Nucl. Sci., vol. 58, no. 1, pp. 194-201, Feb. 2011.
[7] Jinhong Wang, Xueye Hu, Schwarz.T, Junjie Zhu, Chapman.J.W, Tiesheng Dai, Bing Zhou "FPGA Implementation of a Fixed Latency Scheme in a Signal Packet Router for the Upgrade of ATLAS Forward Muon Trigger Electronics", IEEE Trans. Nucl. Sci., vol. 62, pp 2194-2201, Issue: 5, Oct. 2015.
[8] Sarmah. M. J, Azeemuddin. S, "A Circuit to Eliminate Serial Skew in High-Speed Serial Communication Channels", Circuits and Systems II: Express Briefs, IEEE Trans. vol. 62, pp. 1179-1183 Issue: 12, Dec. 2015.
[9] Cannon. M, Wirthlin. M, Camplani. A, Citterio. M, Meroni. C, "Evaluating Xilinx 7 Series GTX Transceivers for Use in High Energy Physics Experiments Through

Proton Irradition", IEEE Trans. Nucl. Sci., vol.62, pp. 2695-2702 Issue: 6, Dec. 2015.

Ms. Bhagyalaxmiis a PG student studying inDept. of PG studies, M.Tech VLSI Design and Embedded Systems, VTU Regional Centre, Kalaburagi. She has completed her BE in Electronics and Communication from APPA College of Engineering, Kalaburagi.

Dr. BaswarajGadgayis a Research guideand Professor in Dept. of PG studies, M.Tech VLSI Design and Embedded Systems, VTU Regional Centre, Kalaburagi. He has 23 years of teaching experience and has published 15 papers in various international journals and conferences.

Ms. Suman B. Pujari is an Assistant Professor in Dept.of PG studies, M.Tech VLSI Design and Embedded Systems, VTU Regional Centre, Kalaburagi. She has 8 months of teaching experience and has published paper in IJEEE.