ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 5, Issue 8, August 2016

DESIGN AND IMPLEMENTATION OF CMOS PWM TRANSCEIVER BY USING SELF REFERENCED EDGE DETECTION TECHNIQUE

K.MANASA, V.VENKATESWARA REDDY

***Abstract*— A CMOS PWM Transceiver is designed and implemented with the help of self referenced Edge Detection technique. The Transceiver is designed with out the use of Phase locked loop which occupies large area and large amount of Power supply. Edge detection technique contrast the difference between the rising edge and modulated falling edge. The modulated falling edge is delayed by 0.5T in one carrier clock cycle. It accomplished area efficient, high robustness by PWM. The measured results by 0.12µm CMOS technology describe 2-bit communication, with small area 0.003536µm^2, power dissipation is 1.02mw and requirement of power supply is 1.20v. For improving the reliability, error check and correction circuit is implemented and evaluated by 1bit PWM measurement.**

***Index Terms*—. pulse width modulation; self-referenced edge detection; timing error measurement**

I. INTRODUCTION

The physical transfer of data over a point to point or point to multipoint communication channel is called as digital transmission or Data transmission The other name for PWM is pulse duration modulation is defined as a process of converting Analog signal to discrete signal. PWM is used to encode the amplitude of a signal. Power loss in a switching device is very low and it is the main advantage of the PWM

Power loss is defined as the product of voltage and current. PWM also works good with the digital controls due to the nature of on/off usually needs duty cycle VLSI is defined as the process of introducing integrated circuits by combining thousands of transistor based circuits into single chip.

In the 1970's VLSI began to develop complex semiconductor and communication Technology. Time domain circuits are developed due to the requirement of reduced power supply for CMOS device. PWM modulation is widely used in number of applications like wire line transceiver, CMOS imagers and Biosensor arrays. Conventional PWM transceiver is implemented and requires large amount of power supply. Power dissipation should be minimized in VLSI in order to improve reliability addition to reducing package cost.

Designing proposed PWM transceiver with the help of using self referenced edge detection technique. It gains area efficient, and high robustness. The proposed PWM Transceiver contrast the difference between rising edge and modulated falling edge in a clock cycle.

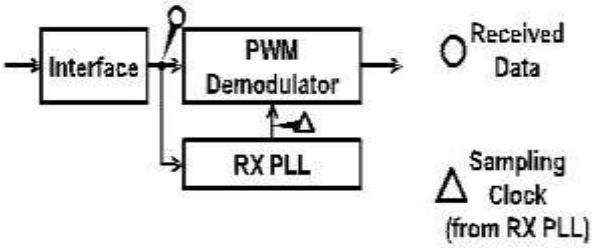

Fig. 1. Conceptual diagram of the conventional PWM receiver in 2-bit PWM.

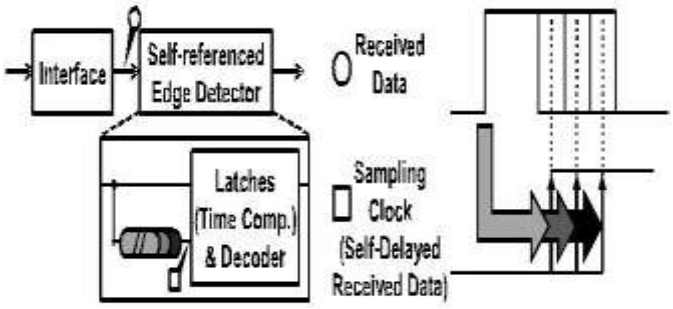

Fig. 2. Conceptual diagram of the proposed PWM receiver in 2-bit PWM.

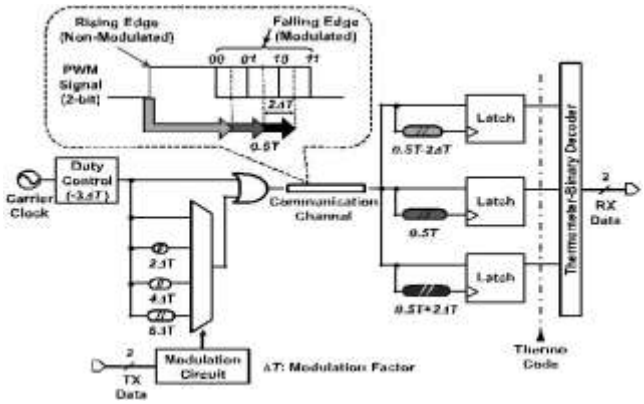

Fig. 3. Circuit implementation of the proposed PWM transceiver architecture in 2-bit PWM.

Manuscript received Aug , 2016.
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ISSN: 2278 – 909X
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Volume 5, Issue 8, August 2016

2 .PWM TRANSCEIVER USING SELF REFERNCED EDGE DETECTION TECHNIQUE

Figs 1 and 2 discussed the conceptual diagram of the conventional and proposed PWM Transceiver. Designing these two circuits for a 2-bit communication. A conventional PWM transceiver requires PLL to generate shifted sampling clocks.

The proposed transceiver consists of latches as timing comparators and a thermometer binary decoder. By contrasting the difference between the rising edge and modulated falling edge in a clock cycle. The proposed method does not require the huge PLL and there by it attains high area efficiency.

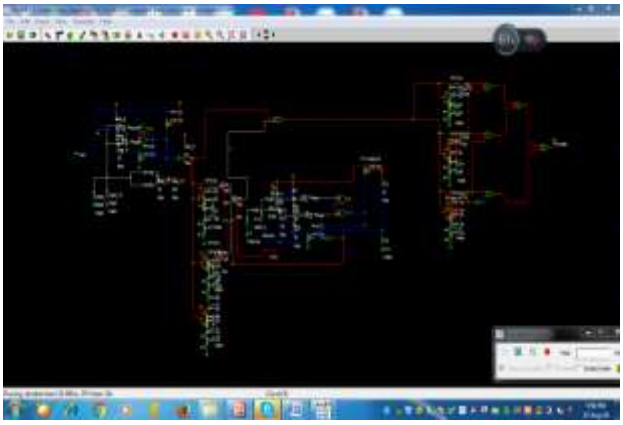


Fig 4: circuit implementation of the proposed PWM Transceiver architecture in 2-bit PWM

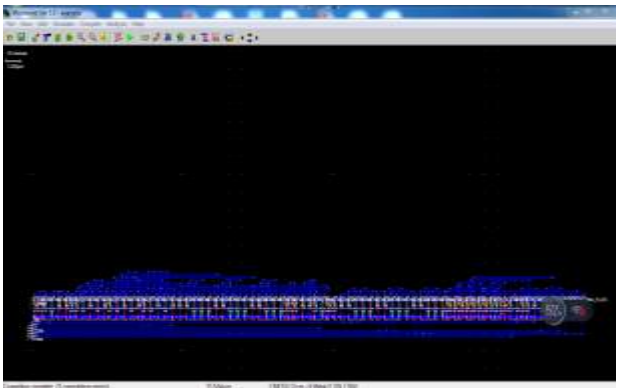


Fig 5: Layout generation of the proposed PWM transceiver architecture in 2-bit PWM

Fig 5 shows the lay out generation of the proposed transceiver architecture in 2-bit PWM. Fig 3 shows that the Transmitter consists of Duty controller, four delay elements with length of multiples of modulation factor, selector controlled by the modulator and OR logic.

The receiver consists of three delay elements with various lengths about a half of the clock period, 0.5T ,latches and a thermometer –binary decoder. The output of the three latches is thermometer codes that are converted to binary code by the thermometer -binary decoder

3 .ERROR CHECK AND CORRECTION CIRCUIT

Error check and correction circuit is essential in order to increase the efficiency of the PWM transceiver with the help of self referenced edge detection technique. Fig 6: shows the diagram of the proposed ECC technique. The auxiliary receiver detects the inter cycle time difference of the adjacent falling edges. The number of cycles are decreases between preceding and succeeding edges due to correlation.

Fig 7 shows the Schematic diagram of the ECC function. Fig 8 shows the layout generation of ECC containing Latches and error detecting logic for 1 bit PWM. By comparing and differentiating from the received data between main receivers and auxiliary receivers

ECC circuit consists of latches and error detector .ECC uses the received data from the main receivers D1, D2 and auxiliary receivers A+, A-.An error code is generated due to the difference between the received data from the main and the auxiliary receiver and that the original bit is inverted..

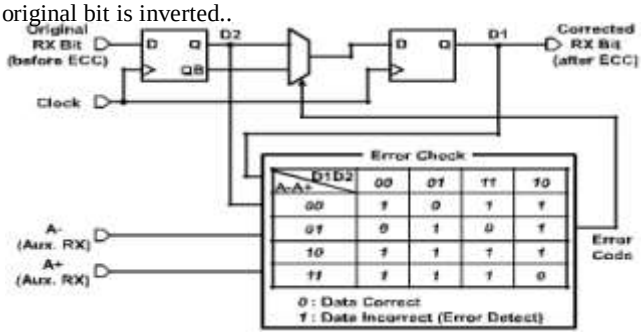


Fig 6: Schematic diagram of ECC containing Latches and error detecting logic for 1 bit PWM.

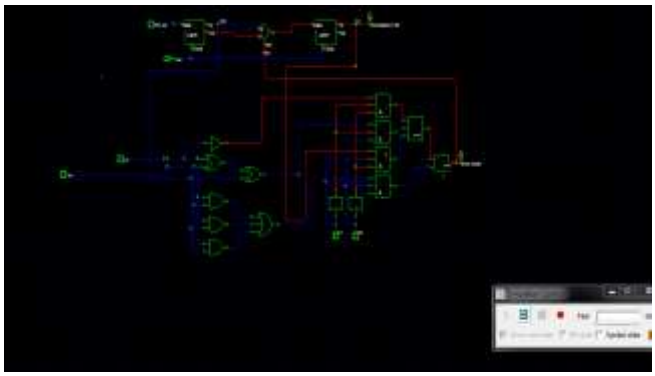


Fig 7: Schematic diagram of ECC containing Latches and error detecting logic for 1 bit PWM

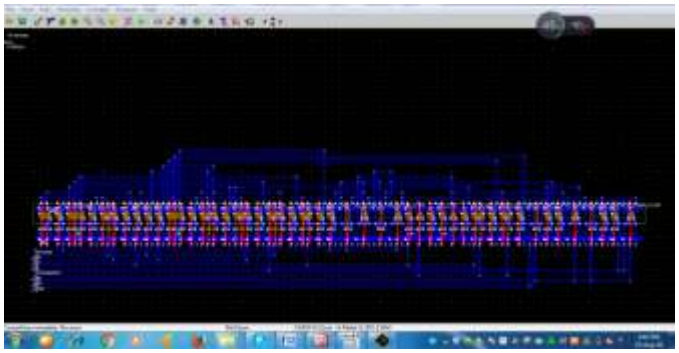


Fig 8: Layout generation of ECC containing latches and error detecting logic for 1 bit PWM

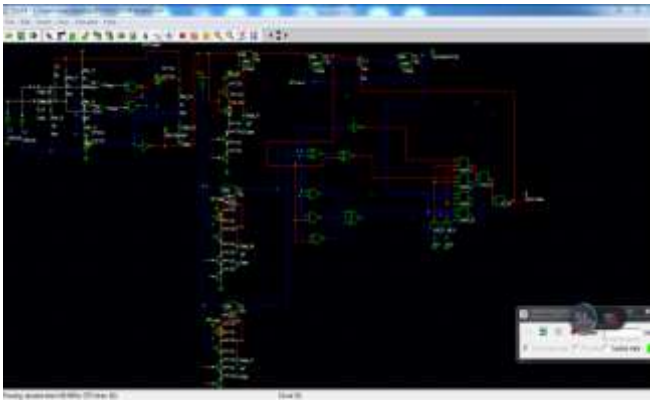


Fig 9 Schematic diagram of the proposed receiver with ECC capability for 1-bit PWM

Fig 8 shows the lay out generation of the proposed receiver with ECC capability for 1-bit PWM and fig 9 shows the schematic diagram of the proposed receiver with ECC capability for 1-bit PWM. The data is compared between from the received data of the main receiver and that of the auxiliary receiver. This technique is flexible under the timing error measurement.

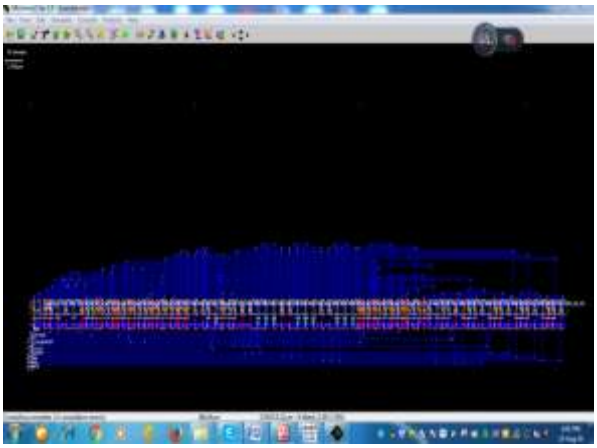


Fig:10 layout generation of proposed receiver

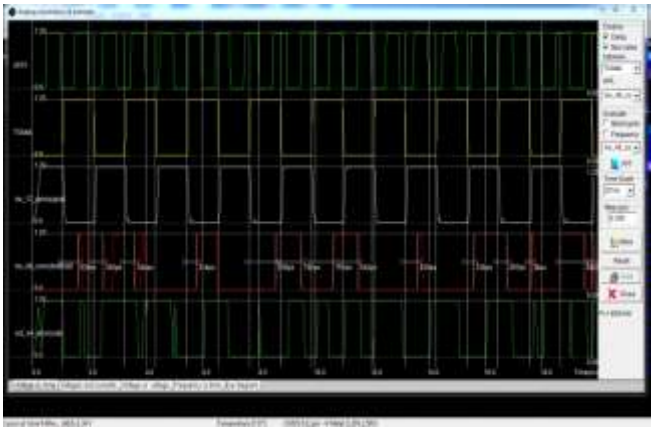


Fig 11 wave forms of the Schematic diagram of the proposed receiver with ECC capability for 1-bit PWM

Fig 11: shows the wave forms of the schematic diagram of the proposed receiver with ECC capability for 1-bit PWM. The error code is generated when there is error code in the transmission of data. The power dissipation of proposed receiver with ECC is 1.654mw, area (A=W×H) W=98µm, H=19µm and power supply is required 1.20 volts by using 0.12µm CMOS technology.

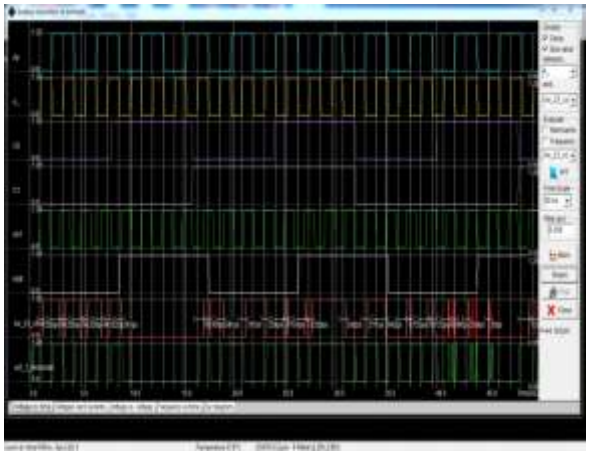


Fig 12 Wave forms of the schematic diagram of the proposed ECC

Fig 12 shows the wave forms of the schematic diagram of the proposed ECC and the power dissipation is 44.19µw, area is W= 54µm, H=15µm and power supply of 1.20 volts by using 0.12µm CMOS technology.

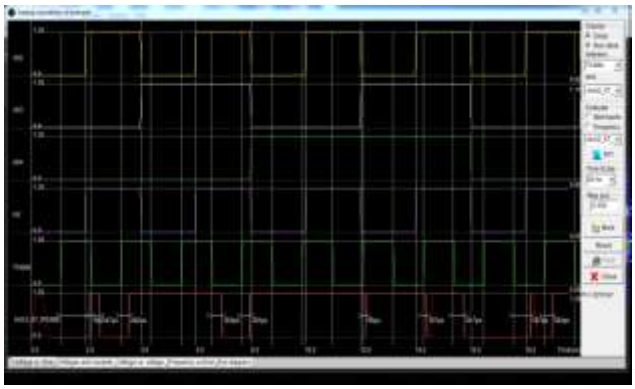


Fig 13 Waveforms of the proposed PWM Transceiver for 2-bit PWM

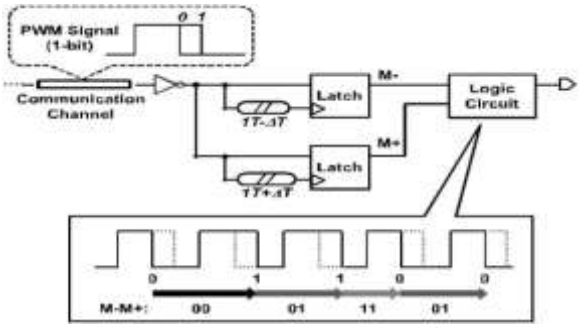
Fig 13 shows the waveforms of proposed PWM Transceiver for 2-bit PWM. The power dissipation is 1.027mw, W=208µm, H=17µm and power supply is 1.20 volts.

4. MEASUREMENT RESULT

The measurement results of implemented CMOS PWM transceiver are Small area (0.003536µm^2), less amount of Power supply is 1.2V and less power dissipation is 1.027mw by using 0.12µm CMOS technology.

5. ANOTHER METHOD

Another method of the Proposed CMOS PWM Transceiver Using Self-Referenced Edge Detection



This circuit diagram introduces another method of the proposed CMOS PWM transceiver using self-reference edge detection technique. In this method it uses only either rising or falling edges. This method reduces the limitation and leads to the application of proposed technique

TABLE 1

6. PERFORMANCE SUMMARY

	This work	Conv.[1] (IEEE 2015)	Conv.[2] (JSSC 2001)	Conv.[3] (JSSC 2007)	Conv.[4] (TIM 2008)
Area	0.003536µm^2	540µm^2	354,444µm^2	14,359µm^2	4,103,532µm^2
Technology	0.128 µm	65nm CMOS	0.25µm CMOS	0.18µm CMOS	0.18µm CMOS
Power supply	1.20v	1.20v	2.5v	1.2v	1.8v
Power dissipation	1.027 mw	3.12mw	66.5mw	3.12mw	3.12mw
Feature	Without PLL	Without PLL	With PLL	With DLL	With PLL

7. CONCLUSION

A CMOS PWM transceiver was designed and implemented with the help of self referenced edge detection technique. While implementing and designing it has the with the following results area 0.003536µm^2 and with a power supply of 1.20 volts ,power dissipation is 1.027mw by using 0.12µm CMOS technology.

8. REFERENCES

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