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A Redundant BCD Codes Based High Speed Radix-10 Multiplication

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***Abstract*— In digital systems Decimal hardware implementations have recently gained importance because they provide higher accuracy in finance, commercial, and internet based applications. The objective of the project is to speed up the BCD parallel multiplier by using redundancy of two decimal representations: Redundant BCD representation (XS-3) and the ODDS (overloaded decimal digit set) representation. The proposed method reduces the latency of Digital floating point units. The implementing system goes through mainly three stages: one is Generation of partial products, it generates multiplicand multiples and uses SD Radix-10 recoding table (MBE scheme) for multiplier that gives less number of partial products. Next stage involves Reduction of partial products to two 2d-digit words by using CSA tree, which increases the speed of operation. Last stage involves final addition using BCD adder. This method can implemented for m × n multiplication where m and n are extended up to 128 bits. The proposed BCD parallel multiplier improves the efficiency of BCD encoding and reduces the overall multiplier area and latency of DFPU's.**

***Index Terms*— Decimal floating point unit, Booth encoder, Decimal multiplication, redundant decimal representation, overloaded decimal representation.**

I. INTRODUCTION

Decimal floating point numbers and Decimal fixed point numbers have a great significance in finance, commercial and internet based applications. In fixed point, conversions and rounding errors can be tolerated easily where as in case of floating point numbers these conversions and rounding errors cannot be tolerated easily. For that IEEE 754-2008 standard provides a format and specification for decimal floating point arithmetic. So it has encouraged a significant amount of research in decimal hardware and software. In digital floating point units multiplication and division are performed iteratively by means of digit by digit algorithm, so they present poor functioning. For reducing the latency of decimal floating point units we are going to use parallel techniques.

In general decimal hardware in digital systems uses BCD encoding in place of binary encoding for easy transformation between user and machine.

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BCD converts a number P in decimal format with each digit Pi ∈ [0, 9] only; So BCD encoding is less economic because the code 10 to 15 is not used. Hence there is a need to improve efficiency of BCD encoding.

The melioration of BCD parallel multiplication by using redundancy of two decimal representations: Redundant BCD representation (XS-3) and the ODDS (overloaded decimal digit set) representation, improves the performance of parallel multiplication. Since the Redundant BCD representation (XS-3) is a self complimenting code, so the negative multiplicand multiples can be obtained by just inverting its bits as in binary. The main aim is to speed up multiplication and other objectives are

- To nullify long carry-propagation in the generation of multiplicand multiples.
- To get the negative multiplicand multiples from positive ones easily by using self complimenting code.
- To simplify the recoding of the multiplier value for effective partial product reduction.

II. LITERATURE SURVEY

Vazquez A, Antelo, Montuschi et al[2], explains the High performance parallel decimal multiplication Based on the redundant binary representations 4221, 5211. The partial product generation stage goes into more complicate while calculating 3X multiple, and also rounding errors may take place.

Yeh c.Jen et al [3], explicate the introductory of Booth encoded parallel multiplier based on the modified booth encoding algorithm. In this method the partial product generation stage includes two more logics while calculating negative multiplicand multiples. Hence the power dissipation and total chip area increase rapidly while designing modern parallel decimal multipliers. Cowlishaw F.M et al [4], explicate the decimal floating point algorism. Different rules in this algorism explain the standardization and normalization of decimal floating point arithmetic. For modern designs of Decimal floating point unit those rules gives conversion and rounding errors.

III. RADIX-10 PARALLEL DECIMAL MULTIPLIER

i. SD Radix-10 Architecture: The architecture of Radix-10 for p-digit BCD parallel multiplication is based on the method for generation of partial products and reduction severally. The codification 5211 and 4221 is used in place of

BCD to present the partial product is principal aim of this architecture. This amends the partial product reduction w.r.t to other methods, in price of response time and area as excepted. The architecture of p-digit SD Radix-10 multiplication involves in three steps, Partial product generation, Reduction of partial products and final BCD sum.

ii. Generation of partial products: Generation of p+1 partial product is performed by recoding of multiplier value using SD-Radix-10 re-coder and generation of multiplicand multiples. Each recoded multiplier bit checks a level of 5:1 multiplexer which takes a multiplicand multiple (0X, 1X, 2X, 3X, 4X, 5X) coded in 5221. To get each multiplicand multiple a level of XOR gate negates the resultant bit of the 5:1 multiplexer when the sign of respective multiplier value is negative. To reduce the p+1 partial products coded in 4211, first the partial products are arranged according to the respective decimal weights. The ith column of the partial product array is reduced using i:2 CSA tree into two digits. These digits varies from i= d+1 to i=2 for each column. Hence the d+ 1 product is minimized to two 2d digit operands S and C coded in 4221.

The final output is P = 2C+S. this architecture has less latency and takes less equipment than other choices.

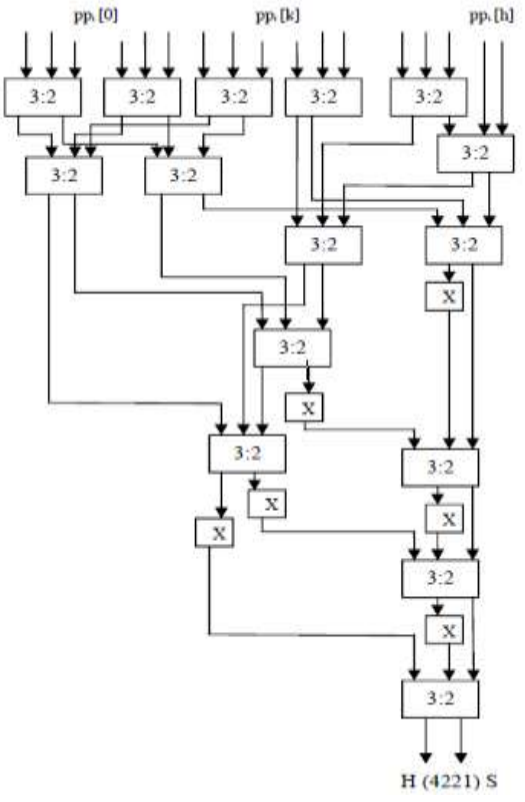


Fig 1: i : 2 CSA tree

iii. Reduction of partial products: The array of partial products produced by the SD Radix-10 recoding, each column of p digits is reduced into a decimal digit by i: 2 CSA tree as shown in figure 1. The carries produced in between columns are passed to final sum in carry save addition.

The use of 4221 and 5211 coding for partial products reduces the area and delay. These codes eliminate the necessity of decimal corrections. But the i:2 CSA tree has long carry propagation for the digits coded in 4221. Hence the area and delay is more in this system.

IV. IMPLEMENTATION

The architecture and algorithm of BCD parallel multiplication efforts some attributes of two distinct redundant BCD representations to speed up the calculations are redundant BCD representation (XS-3), overloaded BCD representation (ODDS). Suggested methods are developed to reduce the area and latency of former high performance executions.

i. Generation of partial products: Partial product generation includes parallel generation of partial products, including recoding of the multiplier value and calculation of multiplicand multiples. The positive multiplicand multiples (0X, 1X, 2X, 3X, 4X, 5X) coded in XS-3 has many advantages.

By using XS-3 we get the negative multiplicand multiples from positive ones easily, because it is a self complimenting code. The usable redundancy allots nullification of long carry propagation in the generation of multiples.

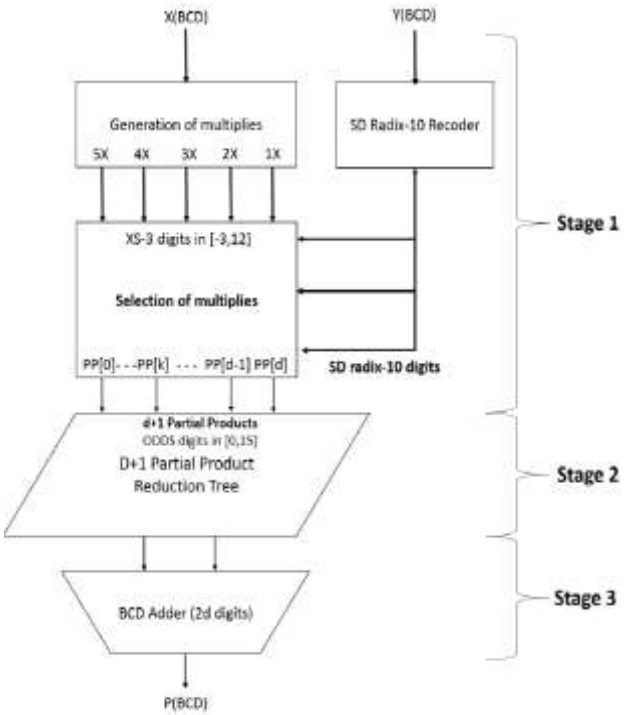


Fig 2: Combinational SD Radix-10 Architecture

The overloaded decimal digit set takes similar 4-bit binary codes as non redundant BCD techniques. Different kind of formats and arithmetic has been aimed to amend the performance of BCD multiplier.

In digital floating point units, multiplication and

division are executed iteratively by means of digit by digit algorism. For reducing the latency of decimal floating point units here we are using parallel techniques. Carry save format representation of BCD presents a radix-10 operand using a carry bit and BCD digit at each decimal.

ii. Sign digit Radix-10 generation:

Generation of partial products comprises, calculating multiplicand multiples and recoding of the multiplier value using SD Radix-10 recoder. The recoding table consists d SD Radix-10 digits Ybk [-5,5], with k=0,1,2,…..d-1, Yd-1 as MSD.

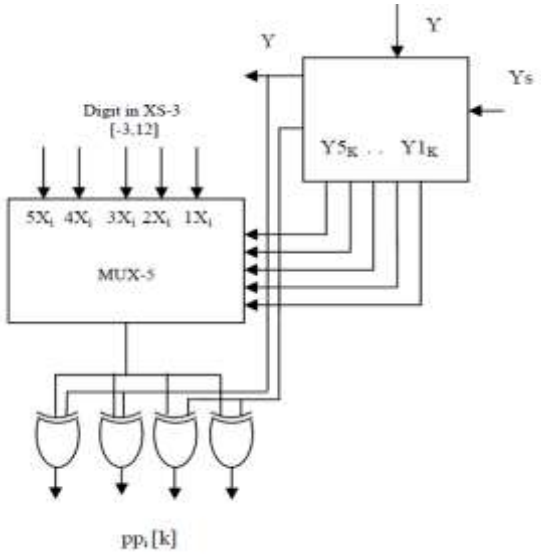


Fig 3: SD Raix-10 generation of partial products

Each digit Ybk is denoted with 5 bit hot-one-code (Y1k, Y2k, Y3k, Y4k, Y5k) to choose corresponding { 1X, 2X, 3X, 4X, 5X } with a 5:1 multiplexer and a sign bit Ysk that represents the negation of chosen multiple as shown in fig3. The negative multiplicand multiples are found by Ten's complementation of positive ones. This is similar to carrying the Nine's compliment of the positive ones and then adding 1. By using XS-3 code the Nine's compliment can be easily obtained by simple bit inversion.

Partial products PP[d-1], …, …, …., PP[0] are produced by Ybk using 5:1 multiplexer. XOR gates at the output side of fig 3 invert the multiplicand multiple to get it's nine's compliment, if Ysk=1. In other words if the bits Y1k, Y2k, Y3k, Y4k, Y5k are all zero then PP[k]=0, but it has to be 0011 as encoding of XS-3. To make the two least significant bits to 1 take the input of XOR gate as Ysk*= Ysk ∨ Ybk. Here ∨ operator denotes the Boolean OR operator. The most significant partial product PP[d] depends on Ysd-1 only.

iii. Reduction of partial products:

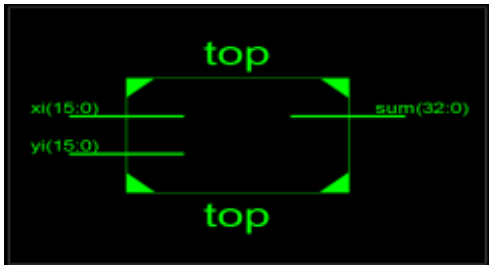
Partial product reduction tree comprises of three stages, Binary CSA tree to calculate partial product sum in binary carry save form (S,C). A Sum correction block is used to count the carries that are generated between the digit 3:2 compressors. In order to obtain the final double word product (A,B), sum correction block increments the carry save sum according to the carries count.

At last the addition of digits Gi, Zi, Wzi of the each column, Gi+Zi+Wzi ∈ [0, 45]. Decimal 3:2 digit compressor reduces digits Wzi, Gi,Zi in to two digits Ai, Bi. The final product can be obtained by performing single BCD carry save propagate addition P=A + B. This is last stage in multiplication. Here Ai + Bi ∈ [0, 18].

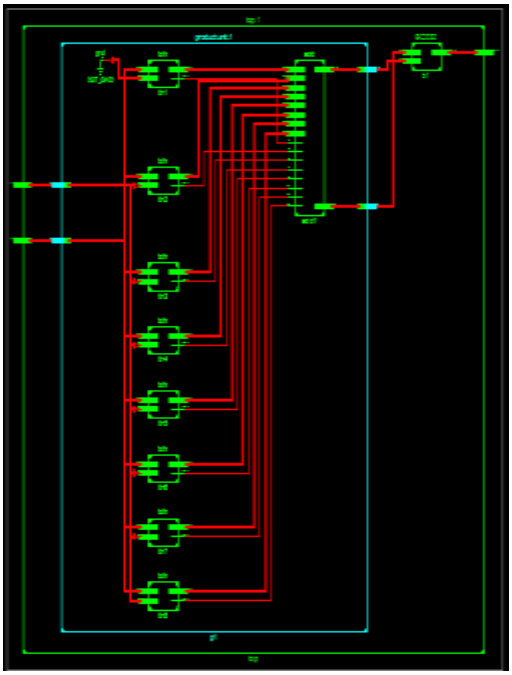
V. SIMULATION OUTPUTS

1. 16 bit multiplication (Existing):

Multiplication unit is projected and applied in verilog HDL. Its model output is shown in figure. Consider Xi and Yi are two decimal numbers, where I ∈ (0,15) and Pi is the final output sum.



A)



B)

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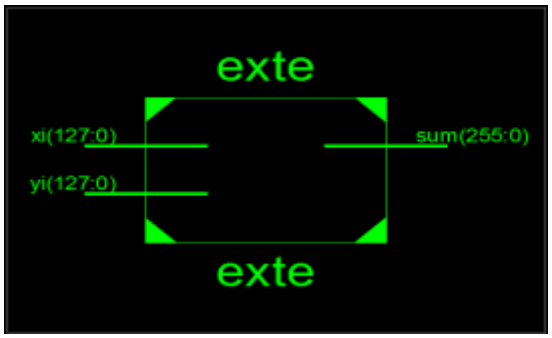
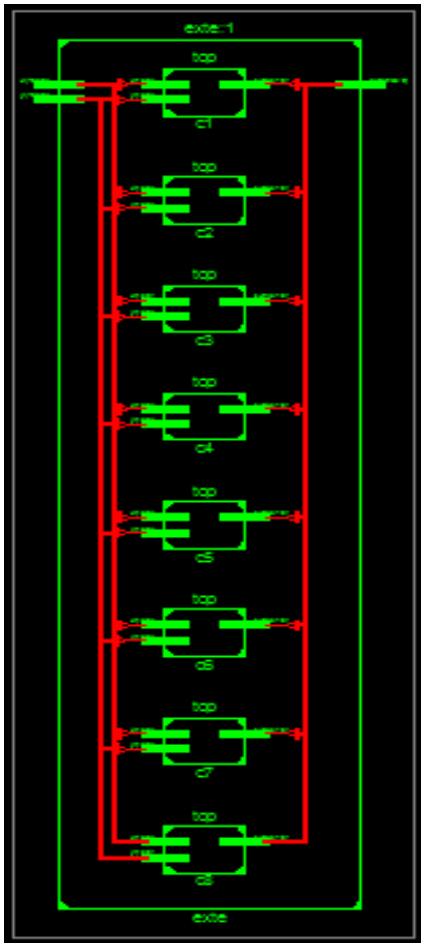
C)

Fig: 3 A) Block diagram B) RTL schematic C) Wave form

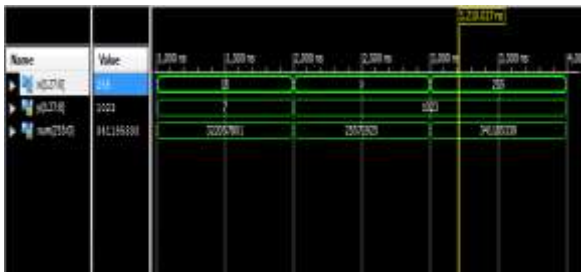
2. 128 bit multiplication (Proposed):



A)



B)



C)

Fig: 4 A) Block diagram B) RTL schematic C) Wave form

PERFORMANCE COMPARSION:

A. Existing:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	349	960	36%
Number of 4 input LUTs	644	1920	33%
Number of bonded IOBs	64	66	96%
Number of MULT18X18SIOs	2	4	50%

```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 53.034ns
```

Fig: Area and Delay for Existing method

B. Proposed:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	3444	960	358%
Number of 4 input LUTs	6352	1920	330%
Number of bonded IOBs	512	66	775%

```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 52.216ns
```

Fig: Area and Delay for Proposed method

V. CONCLUSION

Redundant BCD codes based High speed radix-10 multiplication was implemented. The results were compared for both existing and proposed methods. From the received results, it is clear that the proposed decimal multiplier gives reduced delay and area because of redundant BCD representations. Applying this radix-10 multiplier in FIR systems gives best results and is used as high speed applications of DSP and can also be implemented in FPGA.

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