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REVIEW PAPER ON AREA EFFICIENT BCD MULTIPLIER AND MODIFIED BINARY TO BCD CONVERTER

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Abstract- Decimal data processing applications have grown exponentially in recent years thereby increasing the need to have hardware support for decimal arithmetic. Binary to BCD conversion forms the basic building block of decimal digit adder [1-2]. This paper presents novel high speed low power architecture for binary to BCD conversion which provides better results in terms of power, area, and delay than the existing designs of binary to BCD converter and area efficient BCD multiplier.

INDEX TERMS:- Add-3 algorithm, BCD converter and array multiplier, Finite State Recorder, and BCD multiplication.

I. INTRODUCTION

The center of any kind of digital processor and micro processor is its data path. Data path is one of the critical components which decide the key parameters of their design such as the clock frequency, area and power dissipation look up table of the design. Adders and multipliers are the foremost components in the data path and they are of major anxiety for any digital designer of the data path. The use of IP being popular for designing outsized systems, it is of more significance to consider the presentation of various digital adder and digital multiplier implementations that are offered with the commercially available IP. This paper is addressed on analyzing digital Adders and that are available to design with VHDL. Decimal data processing applications have matured exponentially in modern years thereby increasing the necessity to have hardware and software support for decimal arithmetic [3-4]. Decimal Arithmetic is receiving noteworthy attention in marketable business and internet stand applications, providing hardware and software support and in this direction it is hereafter that necessary calculations done is of saleable, scientific and of financial use.

II. PROPOSED WORK

The first approach is a binary to BCD adder using a novel Double Digit Decimal Adder (DDDM) technique. The following section explains the proposed algorithm used in this paper. Simultaneously a novel design for BCD digit multiplication that reduces the critical path and area is also presented in this thesis. To approximate the propagation delay of this adder, we ought to look at the most awful case delay more than every possible combination of binary inputs. This is also known as the significant path. Though the shift and add by 3 algorithm is not novel, the architecture implementation using add by constant which ultimately makes it area efficient is shown in figure 2.The main goal of proposed algorithm is to perform proficient fixed bit binary to BCD conversion.

The binary to BCD can be designed using iterative and add-3 approaches This paper presents two novel techniques for binary adder one is Binary to BCD conversion by add-3 algorithm and another is BCD multiplication in which partial steps are reduced through Finite state machines and Binary multiplication is also done through Double dabble or add-3 algorithm and converted into BCD. The main motive of the proposed algorithm is to execute significantly capable fixed bit binary to BCD conversion in terms of delay, power and area.

BCD ADDER

The proposed algorithm has been intentionally designed for such converters. Most of the newly proposed adder use 16-bit binary to BCD converters. The proposed algorithm has been intentionally designed for such converters. The following section explains the proposed algorithm used in this paper.

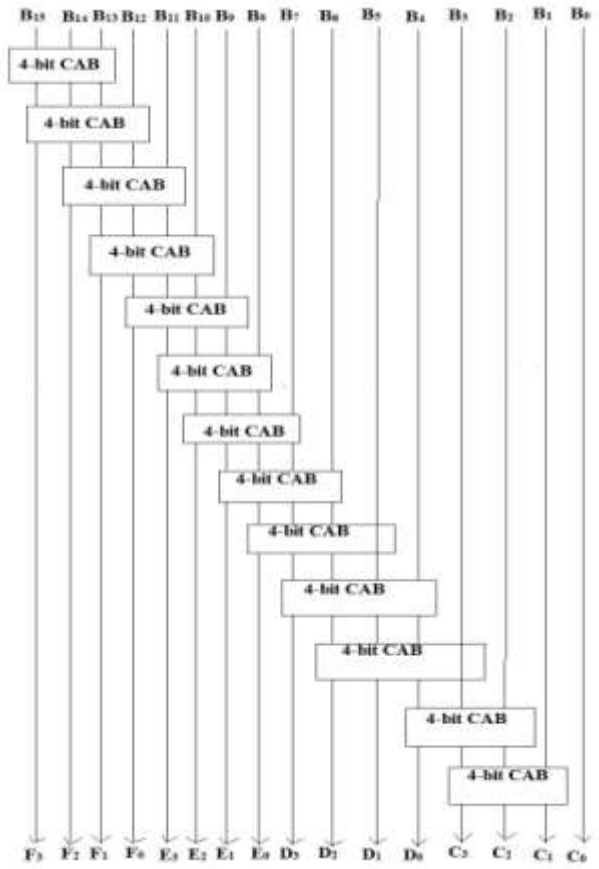

Fig.1. Proposed Shift Add by Constant Architectural Implementation of BCD Converter

Fig.2. shows the architectural implementation of 16 bit Binary to BCD conversion process through Shift Add by Constant mechanism. Here CAB stands for Conditional Adder Block. Most of the newly

proposed adder use 16-bit binary to BCD converters.

BCD MULTIPLIER

High speed computing has become an expected norm for the average user. This has led to increased research efforts in enhancing computing capabilities of a digital circuit. Multipliers are the key components of many high performance systems such as microprocessors, digital signal processors and many countless applications. Multiplication comprises of two stages: Evaluation of partial products and the addition of evaluated products to obtain the final product. These two stages require an efficient adder in order to implement multipliers. As stated earlier the importance of efficient implementation of multiplication unit, there are various measures taken to improve the methods of partial product generation and their accumulation. In this sequence an improved version of parallel decimal multiplication was proposed.

The architecture comprises of following levels:

• Evaluation of decimal partial products.

• Reduction of evaluated products.

• BCD Conversion

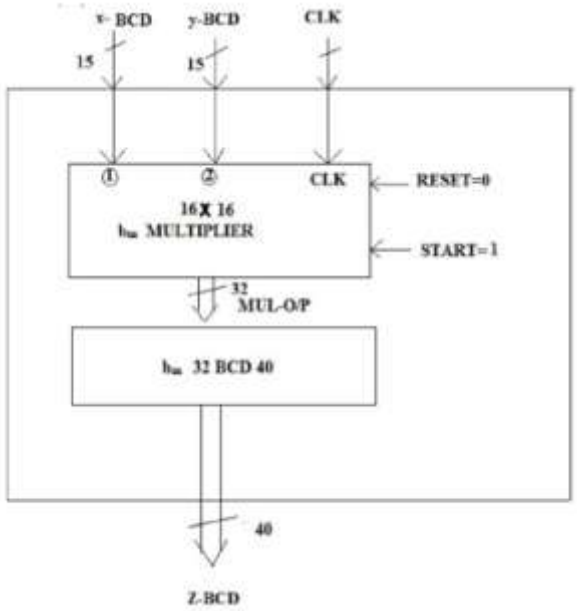

Fig.2. Proposed Architectural Implementation of BCD Multiplier

III. LITERATURE SURVEY

IEEE standard for floating-point arithmetic IEEE SC, Oct.2006 [1] .Here the focus is on the rising appreciation of decimal computer arithmetic in scientific, commercial, financial and Internet-based applications; the only hardware realization of decimal arithmetic algorithms is in advance more importance. Thus Hardware decimal arithmetic units now help as an essential part of some newly commercialized general purpose processors, on the other hand complex decimal arithmetic operations, such as multiplication, have been recognized by somewhat slow iterative hardware algorithms. Nevertheless, with the fast improvements in

very large scale integration (VLSI) technology, semi- and fully parallel hardware decimal multiplication units are predictable to change shortly. The foremost representation for decimal digits is the binary-coded decimal (BCD) encoding. The BCD digit multiplier can help as the significant building block of a decimal multiplier, regardless of the degree of parallelism. A BCD-digit multiplier yields a two-BCD digit product from two input BCD digits. We make available a novel design for the former, showing some benefits in BCD multiplier implementations. ISSN (Print)

Erle, M.A.; Schwarz, E.M.; Schulte, M.J ,17th IEEE Symposium on Computer Arithmetic, 2005 [2]. Here in this paper they have proposed that a BCD-digit multiplier can assist as the key building block of a decimal multiplier, regardless of the degree of parallelism. A BCD-digit multiplier creates a two-BCD digit product from two input BCD digits. We provide a Performing fast, efficient, binary-to-decimal conversion. With a modest amount of circuitry, an order of magnitude speed enhancement is achieved. This attainment deals a matchless benefit to general-purpose computers needing special hardware to interpret between binary and decimal numbering systems.

Fast and compact binary-to-BCD conversion circuits for decimal multiplication ,Osama Al-Khaleel ,Jordan University of Science and Technology, Irbid, Jordan ; Zakaria Al-Qudah ; Mohammad Al-Khaleel ; Christos A. Papachristou Computer Design (ICCD), 2011. [13]. Here in this paper they have proposed that Decimal arithmetic has received considerable attention recently due to its suitability for many financial and commercial applications. In particular, numerous algorithms have been recently proposed for decimal multiplication. A major approach to decimal multiplication shaped by these proposals is based on performing the decimal digit-by-digit multiplication in binary, converting the binary partial product back to decimal, and then adding the decimal partial products as appropriate to form the final product in decimal. With this approach, the efficiency of binary-to-BCD partial product conversion is critical for the efficiency of the overall multiplication process. A recently proposed algorithm for this conversion is based on splitting the binary partial product into two parts (i.e., two groups of bits), and then computing the contributions of the two parts to the partial BCD result in parallel. This paper proposes two new algorithms (Three-Four split and Four-Three split) based on this principle. We present our proposed architectures that implement these algorithms and compare them to existing algorithms. The synthesis results show that the

Three-Four split algorithm runs 15%faster and occupies 26.1%less area than the best performing equivalent circuit found in the literature. Furthermore, the Four-Three split algorithm occupies 37.5% less area than the state of the art equivalent circuit.

FPGA Implementation of Low Power Hardware Efficient Flagged Binary Coded Decimal Adder K.N.Vijeya kumar V. Sumathy Assistant Professor, Ece, Assistant Professor, Ece, Anna University Of Technology, Government College Of Technology, Coimbatore [14]. This paper presents a novel architecture for hardware efficient binary represented decimal addition. We extend the two operand ripple carry addition by one with the third input being constant. The addition technique is made fast by generating flag bits appropriate to the constant added. The third constant in case of our proposed design is 6(0110) for converting the outputs exceeding 9 to Binary Coded Decimal (BCD) number. The proposed BCD adder has been designed using VHDL code and synthesized using Altera Quartus II. Experimental results show that the proposed design outperforms the previous researches in terms of power dissipation and area.

A High Performance Binary to BCD Converter, A. Hari Priya1 Assistant Professor, Dept. of ECE, Indur Institute of Engineering. and Technology, Siddipet, Medak, India [15]. Here they have proposed that the Decimal data processing applications have grown exponentially in recent years thereby increasing the need to have hardware support for decimal arithmetic. Binary to BCD conversion forms the basic building block of decimal digit multipliers. This paper presents novel high speed low power architecture for fixed bit binary to BCD conversion which is at least 28% better in terms of power-delay product than the existing designs. 8.

FPGA Implementations of BCD Multipliers

G. Sutter1, E. Todorovich1, G. Bioul2,3, M. Vazquez,2,3, J-P. Deschamps2,4 —This paper presents a number of approaches to implement decimal multiplication algorithms on Xilinx FPGA's. A variety of algorithms for basic one by one digit multiplication are proposed and FPGA implementations are presented. Later on N by one digit and N by M digit multiplications are studied. Time and area results for sequential and combinational implementations show better figures compared with previous published work. Comparisons against binary fully-optimized multipliers emphasize the interest of the proposed design techniques.

A Parallel Decimal Multiplier Using Hybrid Binary Coded Decimal (BCD) Codes.

Xiaoping Cui, Weiqiang Liu and Dong Wenwen —A parallel decimal multiplier is proposed in this paper to improve performance by mainly exploiting the properties of three different binary coded decimal (BCD) codes, namely the redundant BCD excess-3 code (XS-3), the overloaded decimal digit set (ODDS) code and BCD-4221/5211 code; hence this design is referred to as hybrid. The signed-digit radix-10 recoding with the digit set {-5, 5} and the redundant BCD excess- 3 (XS-3) representations are used for partial product (PP) generation. In this paper, a new decimal partial product reduction (PPR) tree is proposed; it consists of a binary PPR tree block, a nonfixed size BCD-4221 counter correction block and a BCD-4221/5211 decimal PPR tree block. Analysis and comparison using the logical effort model and 45 nm technology show that the proposed decimal multiplier is faster compared with previous designs found in the technical literature.

Implementation of High Speed Radix-10 Parallel Multiplier using Verilog Sonam Negi Pitchaiah Madduri M. Tech VLSI Student, Dept. of ECE This paper delivers the design and implementation of 16-Bit multiplication unit. The design entry is done in Verilog Hardware Description Language (HDL) and simulated using ISIM Simulator. It is synthesized and implemented using Xilinx ISE 12.2. Synthesis results have shown that 20.3% reduction in 4-Input LUTs and 20.4% reduction in the number of slices is observed in the modified methodology. Further 11.5% reduction of maximum combinational path delay is also observed in the modified architecture, thereby leading to high speed multiplication for VLSI applications.

IV. CONCLUSIONS

A Novel integrated BCD/ Binary multi-operand addition and multiplication algorithm is performed. The binary parallel multi-operand addition and mulptilication is to be used by programmers to convert a binary number to decimal. It will be performed by shift and add by 3 algorithms, and can be implemented by using a less number of gates in computer hardware, which ultimately makes it area efficient.

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