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AREA EFFICIENT BCD MULTIPLIER AND MODIFIED BINARY TO BCD CONVERTER

Poornima Shrivastava[1] , Prof. Balram Yadav[2]

[1,2] Scope College Of Engineering, Bhopal, India

Abstract- In view of increasing eminence of commercial, economic and Internet-based applications that process data in decimal arrangement, Synthesis results for 2, 4, 8, and 12 operands and 8 decimal digits provide useful statistic in formative each adder's performance and scalability. There is a renewed interest in providing hardware support to handle decimal data. In this paper, a new architecture decimal addition of binary coded decimal (BCD) operands, which is the core of high speed multi-operand adders and ,is proposed Simulation results show that the proposed add-3 digit BCD adder achieves an improvement of 40% in delay and another is BCD multiplication in which partial steps are reduce and Binary multiplication is also done through Double dabble or add-3 algorithm and converted into BCD which improves 30-40% in terms of area. This paper delivers the design and implementation of 16-Bit multiplication unit. Both the design entry is done in Verilog Hardware Description Language (HDL) and simulated using ISIM Simulator. It is synthesized and implemented using Xilinx ISE 14.1. Synthesis results have shown that 40% reduction in 4-Input LUTs and 35% and 21% reduction in maximum combinational delay and reduction in the number of slices is observed in the modified methodology. Further reduction of maximum combinational path delay is also observed in the modified architecture, thereby leading to high speed multiplication for VLSI applications.

INDEX TERMS: - add-3 algorithm, BCD converter and array multiplier, Finite State Recorder, and BCD multiplication.

I. INTRODUCTION

Utilization of binary data is very speedy on digital computers. But seeing as, decimal

arithmetic is more beneficial than binary arithmetic operation; the conversion of binary data to BCD data is involved. Decimal multiplication is the fundamental operation for any hardware implementation of decimal arithmetic and it is also a fundamental part to the above mentioned digital decimal-dominant applications Decimal Arithmetic is receiving significant attention in commercial business and internet based applications, providing hardware support in this direction is henceforth necessary. Improving BCD architectures, to enable faster and compact arithmetic. In this paper we introduce a new architecture for binary to BCD Conversion of partial products which forms the core of decimal multiplication algorithms such as [7] and [8]. The speedup, area reduction and power consumption of the proposed architecture is analyzed and comparisons with recent architectures is provided. The current state of art conversion scheme [7] is studied and irregularities in the implementation of their converter have been discussed.

The Results show that the proposed design brings considerable improvement in terms of latency, area and power consumption overview on general BCD conversion and its need. The binary numbering system is, far-off the most ordinary numbering system in use in computer systems in this scenario. In days because of there were all the computer systems that were based on the decimal numbering system slightly than the binary numbering system. Such computer systems were very well-liked in systems generally or for business/commercial systems. And internet based applications, even though systems designers have realize that binary arithmetic is not quite always better than decimal arithmetic for general calculation and application the parable still continue that decimal arithmetic is better for money calculations and some general purpose application than binary arithmetic. as a result, many software systems still identify the use of decimal arithmetic in their calculations [16].BCD demonstration does offer one big advantage over binary representation: it is practically small to convert between the string representation of a decimal number and its BCD representation. This feature is for the most part valuable when working with fractional values since fixed and floating point binary representations cannot exactly represent many

II. PROPOSED ALGORITHM

The first approach has a binary to BCD adder using a novel Double Digit Decimal Adder (DDDM) technique. The following section explains the proposed algorithm used in this paper.

Simultaneously a novel design for BCD digit multiplication that reduces the critical path and area is also presented in this thesis. To approximate the propagation delay of this adder, we ought to look at the most awful case delay more than every possible combination of binary inputs. This is also known as the significant path. Though the shift and add by 3 algorithm is not novel, the architecture implementation using add by constant which ultimately makes it area efficient is shown in figure 3.1.The main goal of proposed algorithm is to perform proficient fixed bit binary to BCD conversion.

The binary to BCD can be designed using iterative and add-3 approaches This paper presents two novel techniques for binary adder one is Binary to BCD conversion by add-3 algorithm and another is BCD multiplication in which partial steps are reduced through Finite state machines and Binary multiplication is also done through Double dabble or add-3 algorithm and converted into BCD. The main motive of the proposed algorithm is to execute significantly capable fixed bit binary to BCD conversion in terms of delay, power and area.

BCD ADDER

The proposed algorithm has been intentionally designed for such converters. Most of the newly proposed adder use 16-bit binary to BCD converters. The proposed algorithm has been intentionally designed for such converters. The following section explains the proposed algorithm used in this paper.

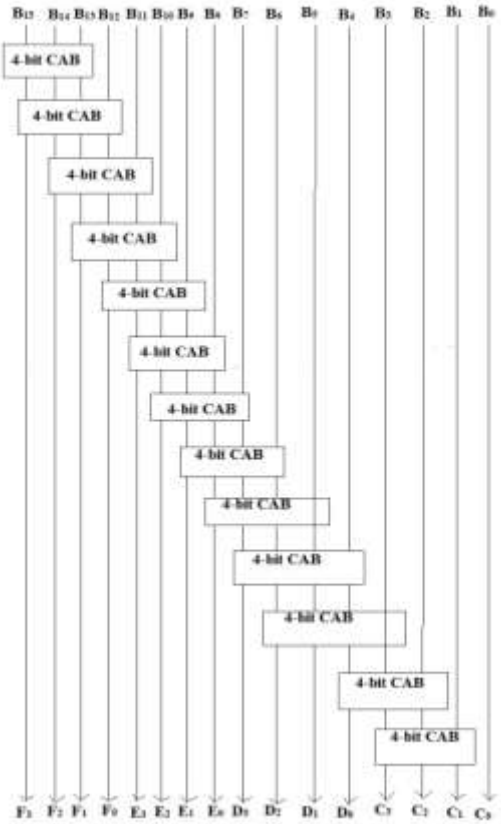

Fig.1. Proposed Shift Add by Constant Architectural Implementation of BCD Converter

Fig.1 shows the architectural implementation of 16 bit Binary to BCD conversion process through Shift Add by Constant mechanism. Here CAB stands for Conditional Adder Block. Most of the newly proposed adder use 16-bit binary to BCD converters.

BCD MULTIPLIER

High speed computing has become an expected norm for the average user. This has led to increased research efforts in enhancing computing capabilities of a digital circuit. Multipliers are the key components of many high performance systems such as microprocessors, digital signal processors and many countless applications. Multiplication comprises of two stages: Evaluation of partial products and the addition of evaluated products to obtain the final product. These two stages require an efficient adder in order to implement multipliers. As stated earlier the importance of efficient implementation of multiplication unit, there are various measures taken to improve the methods of partial product generation and their accumulation. In this sequence an improved version of parallel decimal multiplication was proposed.

The architecture comprises of following levels:

- Evaluation of decimal partial products.
- Reduction of evaluated products.
- BCD Conversion

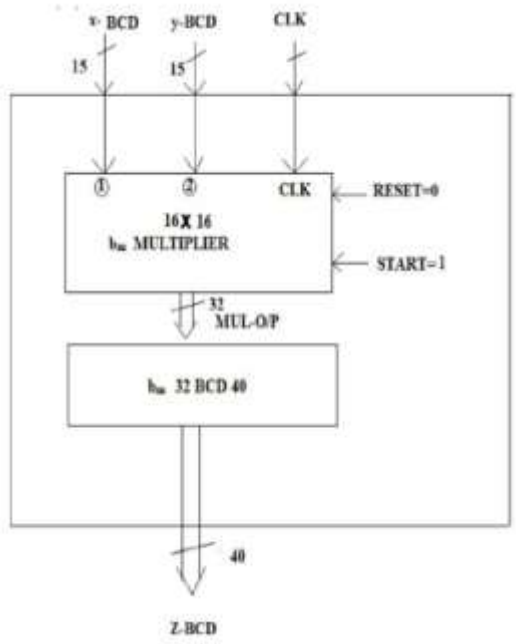

Fig. 2 Proposed Architectural Implementation of BCD Multiplier

Here our proposed work is first to perform binary multiplication and then reducing the partial products after getting output of binary multiplication it I converted into BCD through Double Dabble technique as we can see it in the above block diagram of fig.2.of BCD multiplier

III. SYNTHESISED RESULTS

Execution of 16 bit Binary to Binary Coded Decimal Converter Adder and

Multiplier using add-3 algorithm, has been done using Xilinx 14.1 and simulator has commend out by ISim 14.1e tool. Figures below shows the RTL view of our proposed work that is BCD Adder and BCD Multiplier.

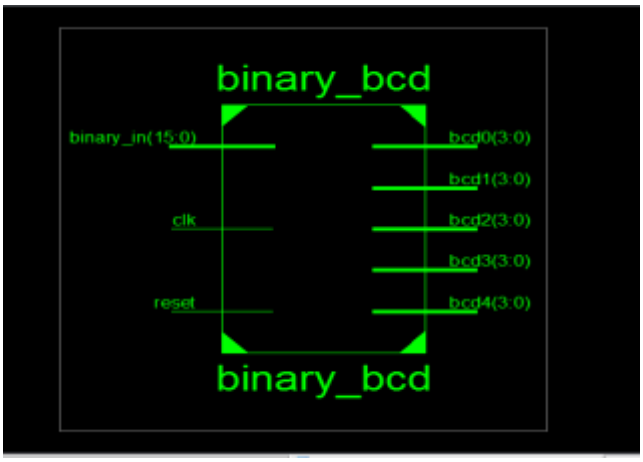

Fig.3 Shown the Input Output RTL view of 16bit BCD Adder

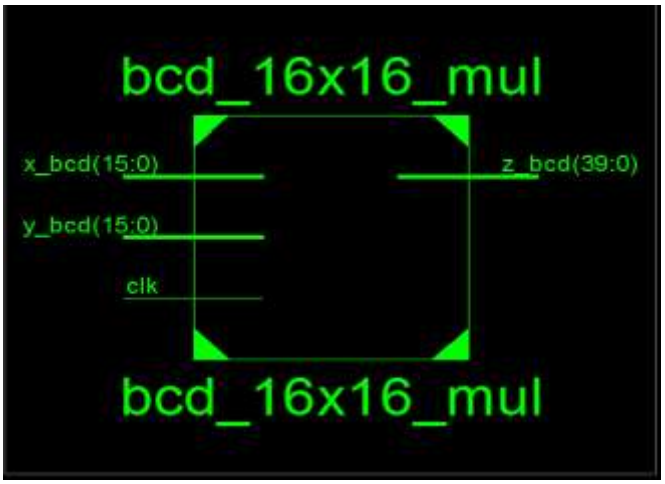

Fig.4 Shown the Input Output RTL view of 32bit BCD Multiplier

Table.1. below shows the comparison of Binary Coded Decimal Converter with existing design. Synthesis results demonstrate that present design causes reduction in delay and area.

TABLE I .Comparison of Proposed BCD Adder

Metric	Area (μm2)	Delay (ns)
Proposed design	48 LUT used ou 63,400 Utilization 1%	1.663
Design [1]	903	1.89

Table.2. below shows the comparison of Binary Coded Decimal Multiplier with existing design [1]. Synthesis results have shown that 40% reduction in 4-Input LUTs and 35% reduction in the number of slices is observed in the proposed methodology.

TABLE.II. Device Utilization Summary of 32-Bit Conventional and Modified Multiplier Architecture

Multiplier	conventional	Modified	proposed
NO. OF 4 INPUT LUTS	2359	1878	1165
NO. OF OCCUPID SLICES	1232	980	659

Further 21% reduction of maximum combinational path delay is also observed in the proposed architecture, thereby leading to high speed multiplication for VLSI applications.

TABLE III. Performance Analysis of 32-Bit Conventional and Modified Multiplier Architecture

Multiplier	Conventional	Modified	proposed
Maximum combinational path delay (ns)	139.40	123.266	97.695
Latency			15 CLK Cycles

IV. SIMULATION RESULTS

This paper delivers the design and implementation of 16-Bit multiplication unit. The design entry is done in Verilog Hardware Description Language (HDL) and simulated using ISIM Simulator. It is synthesized and implemented using Xilinx ISE 14.1 The Binary to BCD converters and Multi-operand designs all the inputs were set to have a clock rate of 100%. Binary to BCD structures based on the proposed algorithm were designed and the Binary to BCD converter in the proposed algorithm was replaced with that of architecture [8] for fair comparisons. As we can see in the figures below are the simulation waveform of BCD adder and BCD multiplier.

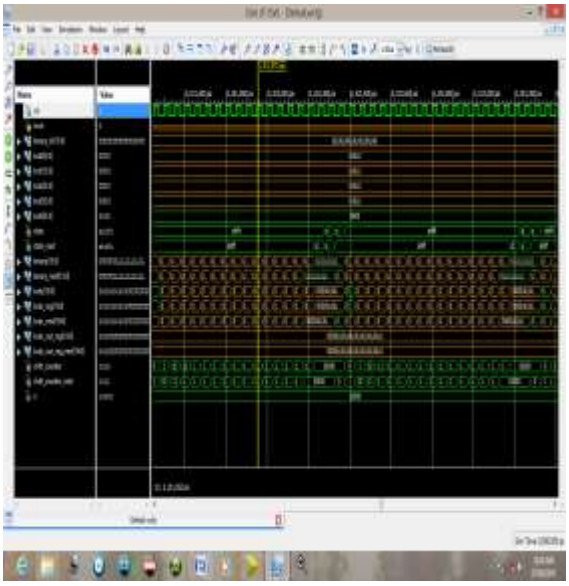

FIG.5 Simulation result of 16 bit Binary to BCD converter

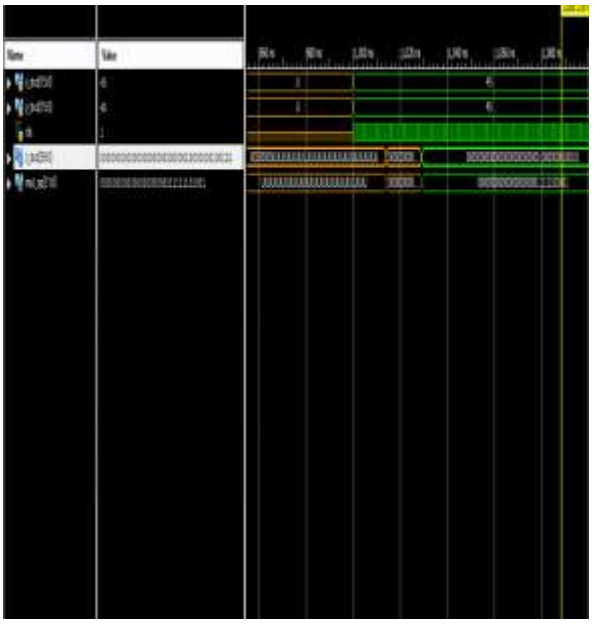

FIG.6 Simulation result of 16bit Binary to BCD multiplier

V. CONCLUSIONS

A Novel integrated BCD/ Binary multi-operand addition and multiplication algorithm is performed. The binary parallel multi-operand addition and multiplication is to be used by programmers to convert a binary number to decimal. It will be performed by shift and add by 3 algorithms, and can be implemented by using a less number of gates in computer hardware, which ultimately makes it area efficient.

In this paper the design and implementation of Finite State Machine parallel decimal multiplier using modified BCD adder is shown for area-efficient applications. The design reduces the complexity of the previous designs which required extra recordings and also reduces the area by eliminating the recoding used for multiple generations. This work can be extended for the implementation of 32 bit, 64 bit and 132 bit multiplication and there is a scope for VLSI application.

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