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Performance Analysis of InGaAs Double Gate MOSFET

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***Abstract*-Technological improvements have been made due to the scaling of device dimensions in order to attain continuous improvements in circuit speed and reduction in size. This rapid miniaturization of Silicon Complementary Metal Oxide Semiconductor technology had become a key to the electronic revolution. But the scaling of gate length posed a great challenge since it lead to decrease in performance in every succeeding generation. So many research works have been done on new device architectures and materials to address this problem. The use of high-k dielectrics can provide the gate with a better electrostatic control over the channel. To achieve the on-current requirements according to the International Technology Roadmap for Semiconductors specifications, it is necessary to replace Silicon by materials with high electron mobility as the channel material. For the 12 nm technology, the best way to achieve the required performance will be the incorporation of high electron mobility materials as the channel. This project work assesses the performance of Double Gate MOSFET at 12nm gate length with InGaAs and Strained Si as the channel materials. A quantum transport is used to simulate the high electron mobility devices. An effective mass approximation is used to model the material parameters. The simulation results indicate that the transistor performed better with Multigate architecture and InGaAs as the channel when compared to Si-based Double Gate Metal Oxide Semiconductor Field Effect Transistor.**

***Index Terms*— MOSFET, S/D extension, Subthreshold Swing and Drain Induced Barrier Lowering.**

I. INTRODUCTION

The rapid growth of the electronics industry is based on the evolution of integrated circuit technology to provide improvements in cost per function as well as performance. Technological advancements have been achieved over the past three decades primarily through the scale-down of device dimensions in order to attain continued improvement in circuit speed and reduction in size (for lower unit manufacturing cost). The most important and fundamental building block of very large scale-integrated (VLSI) circuits today is the metal-oxide-semiconductor field effect transistor (MOSFET). Ideally, a MOSFET has high drive current (when the gate electrode is biased to turn the transistor on) and low leakage current (when the gate electrode is biased to turn the transistor off). As the MOSFET channel length is reduced to 50 nm and below, the suppression of off-state leakage current becomes an increasingly difficult technological challenge that will ultimately limit the scalability of the conventional MOSFET structure. The bulk-Si MOSFET technology finds itself difficult to meet the required performance targets.

In a "bulk-Si" MOSFET, the channel dopant concentration must be increased as the distance between the source and drain junctions decreases in order to avoid electrostatic coupling of the junctions beneath the channel surface. The higher doping results in degraded low-field mobility which further causes lower transistor drive current. For the gate voltage to effectively modulate the channel potential, the gate-to-channel capacitance must be maximized. This has been achieved by reducing the thickness of the gate dielectric so that it is less than 2 nm in the complementary MOS (CMOS) technology. Unfortunately, further reduction in gate oxide thickness is limited due to the drastic increase in gate leakage current caused due to quantum-mechanical tunneling. The double-gate MOSFET structure minimizes short-channel effects to allow for more aggressive device scaling. Recent theoretical studies suggest that double gate devices can meet performance requirements down to 10 nm gate length. In the past, process complexity posed a serious technological barrier to development of double-gate devices.

For digital circuit applications, the future of technology scaling will rest in the ability to control off-state leakage while still maintaining current drive. This will eventually determine the limit of transistor scaling, as proper operation requires that the device be turned both on and off. By studying off-state leakage current, a quantitative estimate of the scaling limit can be obtained for the double-gate MOSFET, which has been shown to be the most scalable transistor design. Because carrier scattering can be ignored at very small channel lengths, the leakage current of a MOSFET in the off state will be comprised of thermionic emission above the channel potential barrier, band-to-band tunneling between the body and drain, and quantum mechanical tunnelling between the source and drain. Reducing the gate length results in increased leakage current due to weakened gate control of the channel. Reducing the body thickness, however, eliminates leakage paths that are far from the gate[5]. Off state leakage current thus decreases and short-channel effects are minimized at small gate lengths. In addition to traditional oxide thickness scaling,

the scaling limit of the double-gate structure is thus very dependent upon the ability to scale the body thickness.

II.ULTRATHIN-BODY DOUBLE GATE MOSFET

The basic design of the UTB MOSFET, as shown in Fig.1, is to use an extremely thin (< 20 nm) silicon on insulator (SOI) film to reduce subsurface leakage paths. Nearly all the leakage current at *Vg*= 0 in the UTB FET flows along the bottom of the body, which is the least effectively controlled by the gate. Therefore, by eliminating the bottom part of the body (i.e., making the body even thinner) the leakage current can be reduced. Thicker, self-aligned source and drain (S/D) structures are required to minimize parasitic series resistance and achieve high drive current [2].

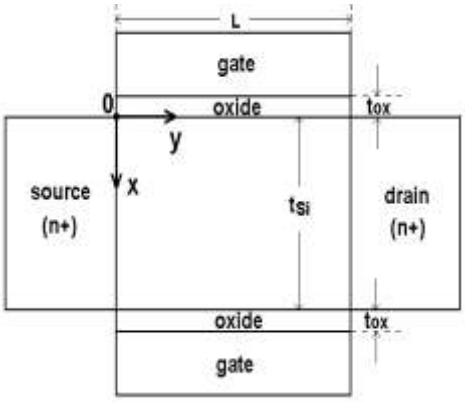


Fig.1 Schematic cross-section of a Symmetrical DG MOSFET

It's impossible to deny that silicon is a successful semiconductor because it forms the key ingredient in any microelectronics industry. However, this material still has its weaknesses, and its MOSFETs are restricted with their relatively slow mobility. III-Vs, such as GaAs, InSb and InAs, are substantially better in this regard, and this advantage has fuelled more than 40 years of development of a compound semiconductor MOSFET. These decades of research have produced several minor successes, but any real progress has been held back by the complexities associated with untangling the underlying physics and chemistry of compound semiconductor surfaces and interfaces[4]\.

The successes obtained with ALD sparked a dramatic growth of the III-V MOSFET community. However, employing an InGaAs channel will provide vast improvements. The bandgap of this ternary can be reduced from 1.42 eV (no indium content) to 0.36 eV (no gallium content), which improves characteristics such as mobility and saturation velocity. A range of inversion-mode surface channel InxGa1–xAs MOSFETs with an indium content, *x*, of 20, 53 and 65% have been built. These transistors, which contain Al2O3, HfO2 and HfAlO dielectrics deposited by ALD, behave in the same way as silicon MOSFETs, but are expected to show a far higher mobility. The inversion with the least amount of indium produces a current of 1 mA/mm, but this rockets to 0.4 A/mm and more than 1 A/mm for MOSFETs with an indium content of 53 and 65%, respectively. In0.65Ga0.35As transistor is the first III-V surface channel MOSFET that is a real field effect device with an inversion current of more than 1 A/mm. It even exceeds the upper measurement limit for a standard semiconductor parameter analyzer, which is 100 mA for a 100 μm wide device[6].

InGaAs FETs most promising characteristic is its ability to scale down to a submicron gate length. Hopefully this scaling will continue down to the length scales associated with silicon MOSFETs, because this would lead to 10 A/mm or 10 mA/μm III-V MOSFETs at a III-V 45 nm technology node However, it is believed that its advances have resulted from an In0.65Ga0.35As channel that has a very high electron mobility and saturation velocity. It is found that the changes in surface potential for strong inversion are much less for InGaAs channels than those made from GaAs. More importantly, In0.65Ga0.35As has a charge neutrality level that is typically just 0.15 eV less than the conduction band minimum. This prevents the buildup of a large number of negative trapped charges at the interface, which can inhibit the introduction of additional inversion carriers by the field effect.

III.DEVICE DESCRIPTION

The device schematics of the double-gate UTB FETs modelled in this work is shown in Fig.2. An In0.75Ga0.25As layer on an In0.52Al0.48As buffer is used as the channel material for III–V FETs. The source and drain regions are n-doped with a donor concentration ND = 5×10^{19} cm−3 and a length of 20 nm. Transport occurs along the <100> crystal axis. The architecture uses an HfO2 high-κ gate stack with a relative dielectric constant ε_R = 20, a thickness t_{OX} = 3 nm, and a conduction-band gap offset ΔEC = 2.3 $In_{0.75}Ga_{0.25}As$[3] .This corresponds to an equivalent oxide thickness (EOT) of 0.585 nm, which is consistent with the International Roadmap for Semiconductors (ITRS) specifications for the 12-nm technology node. The source and drain regions are covered by spacers made of a low dielectric material (ε_R = 5) to reduce the electric fields coupling to the gate. The OFF-state current of all the devices is set to 0.1 μA/μm by varying the work function of the metal gate contact. To reduce the computational burden, the device structures are simulated in two steps. First, only the intrinsic domain, as illustrated in Fig.2 is considered. Then, the source (RS = 80 Ω · μm) and drain (RD = 80 Ω · μm) series resistances taken from the

ITRS are added in a post processing step to the intrinsic *I–V* characteristics.

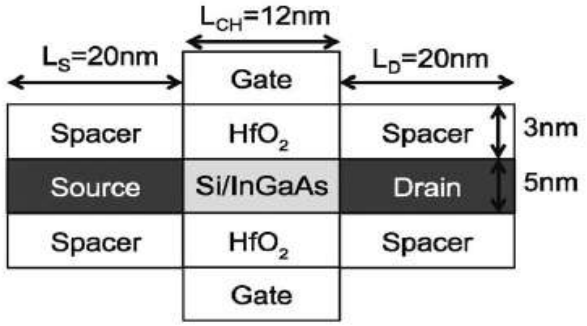


Fig.2 Schematics of the simulated planar UTB DG MOSFET device

The various parameters used for the simulated Double Gate MOSFET are as follows:

The physical structure of the Double Gate MOSFET designed can be described using the dimensions and it is shown in Table 1. The dimensions have their effect on the short channel parameters and the device performance as well. So it's necessary to properly choose the appropriate values to attain the required device performance.

PARAMETER	DIMENSION
Gate length(Lg)	12 nm
S/D extension(Lside)	20 nm
Channel thickness (t_channel)	5 nm
Top oxide thickness(t_top_ox)	3 nm
Bottom oxide thickness(t_bottom_ox)	3 nm

Table.1 Simulated Device Dimensions

The material parameters include the gate material, gate oxide material and the channel material. The material used for the channel is a III-V compound. The various material parameters used are shown in Table 2.

PARAMETER	VALUES
Gate Material:	
Gate work function	4.8 eV
Top Gate Oxide:	
Electron effective mass, m_X,m_Y,m_Z	0.1, 0.1, 0.1
Band gap offset	2.4 eV
Dielectric constant	20
Bottom Gate Oxide:	
Electron effective mass, m_X,m_Y,m_Z	0.1, 0.1, 0.1
Band gap offset	2.4 eV
Dielectric constant	20
Channel Material:	
Electron affinity	4.5 eV
Band gap offset	2.3 eV
Dielectric constant	14.4

Table 2 Simulated Material Parameters

IV.SIMULATION APPROACH

In this work, the real-space quantum transport solver OMEN is used to simulate the 2-D device in the ballistic transport regime. The Schrödinger and Poisson equations are self-consistently solved using the effective mass approximations and a finite difference grid. To account for the nonparabolicity of III–V materials, the effective masses of the $In_{0.75}Ga_{0.25}As$-based transistors are extracted from a sp3d5s* TB band structure calculation including spin–orbit coupling.

The transport effective masses m_t for the $In_{0.75}Ga_{0.25}As$ transistors are obtained by fitting the curvature of the lowest TB conduction band with a parabola. The layers around the $In_{0.75}Ga_{0.25}As$ channel are taken into account when the effective masses are extracted from the TB band structure so that the electron wave function can deeply penetrated into them, resulting into a larger transport effective masses. The Transport and Confinement Effective Masses and Sub band Degeneracy for the $In_{0.75}Ga_{0.25}As$ UTB FET is m_x= 0.059, m_y=0.0109, m_z=0.059

V.RESULTS AND DISCUSSION

The InGaAs DG MOSFET and Si DG MOSFET are simulated and their characteristics are analyzed. Their short channel performance was compared. The Double Gate MOSFET with $In_{0.75}Ga_{0.25}As$ as the channel material is simulated using OMEN_FET to attain better performance than its silicon counterpart. It is simulated in the ballistic regime. The following results indicate the transfer characteristics and output characteristics of this III-V MOSFET which is used for the analysis of the short channel parameters. The transfer characteristics denote the Id-Vg characteristics. Since the simulation domain is restricted to regions surrounding the gate, the Id-Vg curves obtained are the intrinsic characteristics and it has to be post processed with the source and drain resistances, RS= 80 Ω.µm and RD= 80 Ω.µm. The figures shown here are the intrinsic characteristics. The transfer curves are plotted in the semi log scale for the easy analysis of the parameters **Subthreshold Swing, SS** and **Drain Induced Barrier Lowering, DIBL.**

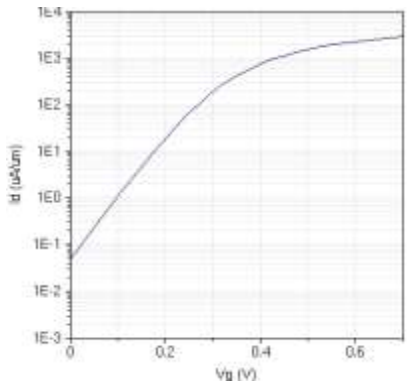


Fig. 3 (a) Intrinsic Id-Vgs characteristics for InGaAs DG MOSFET for Vds= 0.05V(linear case)

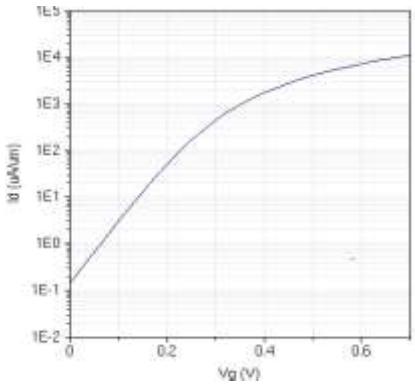
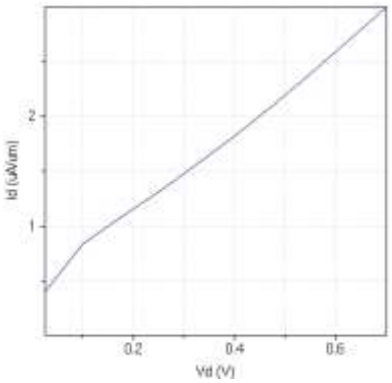


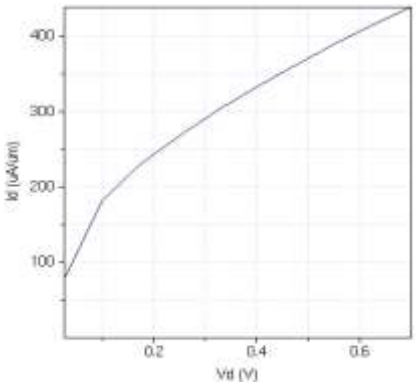
Fig.3 (b) Intrinsic Id-Vgs characteristics for InGaAs DG MOSFET for Vds= 0.7V(saturated case)

The Fig.3 is the transfer curve obtained for the Vdd of 0.7V. This supply voltage is chosen to provide the ON-state performance and threshold voltage as required by ITRS. The Gate voltage is varied between 0V to Vdd and the drain current obtained is plotted against the Gate voltage for two different drain voltages 0.05V and 0.7V which are the linear and saturated voltages respectively. The **threshold voltage** is set to **0.2 V**. The obtained SS value is **85 mV/dec**.The obtained DIBL value for the III-V FET simulated is **90mV/V.**

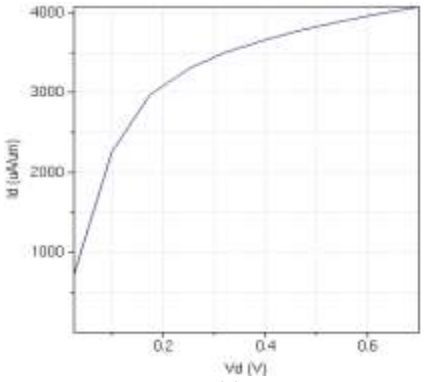
The output characteristics denote the Id-Vd characteristics. The device starts to conduct only on the application of the drain voltage and as the drain voltage increases, the transistor moves from cut-off to linear and then attains saturation. The Fig.4 shows the obtained Id-Vd curve for varying the drain voltage from 0V to 0.7V for different gate voltages.



(a)



(b)



(c)

Fig.4 (a), (b), (c), ID-VDS characteristics of the InGaAs FET at three different gate voltages *VGS* = 0.2V, 0.4V, 0.7V respectively.

The ON-current obtained after post processing with the source drain resistances is I_{on}=1744.56 µA/µm, whereas the intrinsic ON-current was I_{on}=3874.22 µA/µm. Thus it was found that the source and drain series resistances have a negligible effect on the OFF state, but they significantly reduce the drain current in the ON state, by more than 50%.

The Double Gate MOSFET with Silicon as the channel material is also simulated using OMEN_FET. The device is simulated with same parameters and dimensions as that of the III-V FET. The performance parameters taken for the comparison of the InGaAs DG MOSFET and the Si DG MOSFET are SS, DIBL and the I_{ON}. These are the short channel parameters and they determine the device performance. Since the transistors simulated are at a Gate Length of 12 nm, it is crucial to accurately determine the values of these parameters. The Table.3 shows the performance comparison of the simulated devices. It can be understood from the Table.3 that the InGaAs FET performs better compared to the Si FET. The ON-current is much higher for the III-V device than the Si device for the same configuration. Provided a proper processing technology for the III-V FETs, they definitely outperform the Si FETs at the nanoscale with ultra-short gate lengths.

Structure	**Double-Gate**	**Double-Gate**
Material	InGaAs	Si
SS[mV/dec]	85	94
DIBL[mV/V]	90	92
I_{ON}[µA/µm]	1745	634

Table 3 Performance comparison of III-V and Si DG MOSFET

VI.CHANNEL THICKNESS SCALING

The InGaAs-based UTB DG MOSFET is simulated with varying channel thicknesses and the resulting short channel parameters are analysed. Two plots showing the variation of SS and DIBL with respect to the channel thickness, tch, are shown in Fig.5 and Fig.6 respectively.

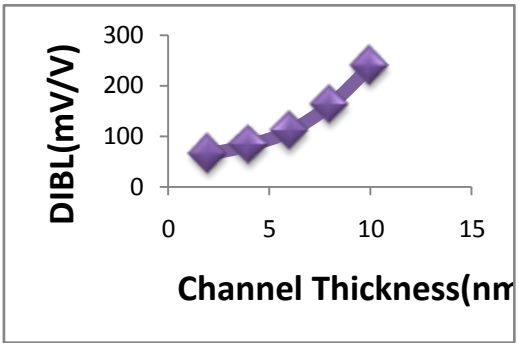


Fig.5 Plot of Channel thickness Vs DIBL

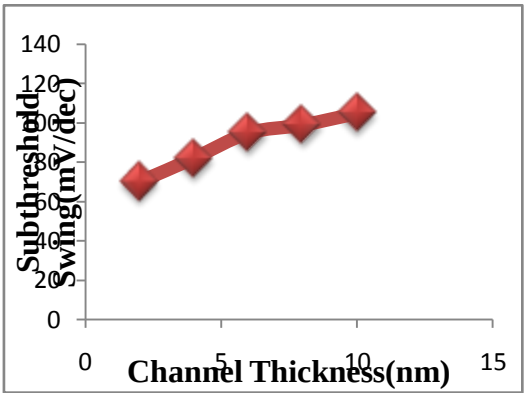


Fig.6 Plot of Channel thickness Vs SS

As the channel thickness increases, the values of SS and DIBL increase as well. Thus it is desirable to reduce the channel thickness to achieve the required performance. Higher gate length to channel thickness ratio results in a stronger gate control of the channel surface potential, which improves SS and DIBL. For a channel thickness of 4 nm, the transistor performs better with SS= 80mV/dec and DIBL = 85 mV/V.

VII.CONCLUSION AND FUTURE SCOPE

A Double Gate Ultra-Thin Body MOSFET with $In_{0.75}Ga_{0.25}As$ and Silicon as the channel materials for a gate length of 12 nm has been simulated and their performances in terms of ON-current, Subthreshold Swing and Drain Induced Barrier Lowering was obtained and compared. It is found that the III-V transistor outperformed the Si transistor in all the aspects and it proved to be a better candidate for

ultra-short gate lengths compared to its Si counterpart. The future work is to devise a FinFET structure for the same gate length of 12 nm with $In_{0.75}Ga_{0.25}As$ and Strained Silicon as the channel materials. The performance can be further improved by incorporating appropriate device scaling.

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