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An Ultra-Low-Voltage Self-Biased OTA for Frequency Response and Gain Improvement

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***Abstract*--This paper present An Ultra-Low-Voltage Self-Biased OTA for Frequency Response and Gain Improvement based low-power low-voltage variant of recently proposed an active element namely Operational Transconductance Amplifier (OTA). The proposed configuration operating at lower supply voltage 0.5 V with the total quiescent power consumption of 2.3738 µW at the biasing current of 4.74 µA. The simulations are performed using Tanner 65nm CMOS technology parameters with 0.5 V supply voltage to validate the effectiveness of the proposed circuit.**

***Index Terms*--Ultra Low Voltage, Bulk-driven MOS Transistor, OTA, Low Power, Analog Circuit.**

I. INTRODUCTION

The trend technology is scaling and demand of portable electronics equipment growing day to day, it has motivated the researcher in developing ultra-low-voltage low-power analog signal processing circuits. Ultra-low-voltage low-power design involves various techniques so that the complete analog circuit could meet the proposed design requirement. Various ultra-low-voltage, low-power design techniques have been reported in many literatures explaining techniques like sub-threshold MOSFETs, level shifter approach, self-biasing cascade approach, bulk driven approach and use of floating gate transistor, and level shifting [1], [2]. Several operational transconductance amplifier (OTA) design that operated from a supply voltage of 1 V or below have been reported [3]-[4]. In this paper, we present an OTA design that operate from a subthreshold 1 V power supply while achieve rail-to-rail input range. The proposed operational transconductance amplifier (OTA) combine two different ultra-low-voltage technique to meet design requirement at the input stage. Mainly, use a two techniques are pseudo-differential amplifiers techniques and bulk-driven MOS transistors, use to achieve rail-to-rail input range with ultra-low-voltage power supply. As novel biasing techniques is also proposed to enhance the performance of the OTAs. Using the proposed techniques eliminate the need for extra biasing circuitry and ensure against process variations under ultra-low-voltage condition. Therefore, the propose techniques enhances the common-mode rejection and power-supply rejection of the OTA.

In this paper is organized as follows: In section II we discuss the design of input stage and techniques used to simultaneously achieve both low supply voltage operations and rail-to-rail input range. In section III can be discuss the proposed biasing techniques and impact of the performance of the OTAs, while in section IV discuss the frequency compensation deployed in the OTA. Section V discussed the circuit design and analysis of the operational transconductance amplifier (OTA) and experimental results concluded the paper.

II. DESIGN OF INPUT-STAGE

Design of input stage with rail-to-rail input common mode range (ICMR) is real challenge low-voltage circuits. Complementary differential pair show in Fig.1. Over entire input range from 0 to VDD, at less-then VDDmin then PMOS complementary differential pair is off, Then two techniques are used. First pseudo differential pair techniques and second bulk-driven MOS transistor techniques. First techniques help reduce minimum limit on operating supply voltage, the second techniques achieve the desire rail-to-rail operations at input.

A. Pseudo Differential Pair

Remove the limit on the operating supply voltage V_{DD}min. Two tail current removing of the pseudo-differential pair then increase the common mode range and output voltage swing. The same time arises two drawback common mode and power supply rejection. Removing two drawback then applying common mode feed forward circuit (CMFF). In addition to save areas and powers with biasing approach, The operational transconductance amplifier (OTA) sensitivity common

mode voltages, supply noises, and process variation is significantly reduce. Fully differential versions of operational transconductance amplifier (OTA) can be built by using replica of second and third stages.

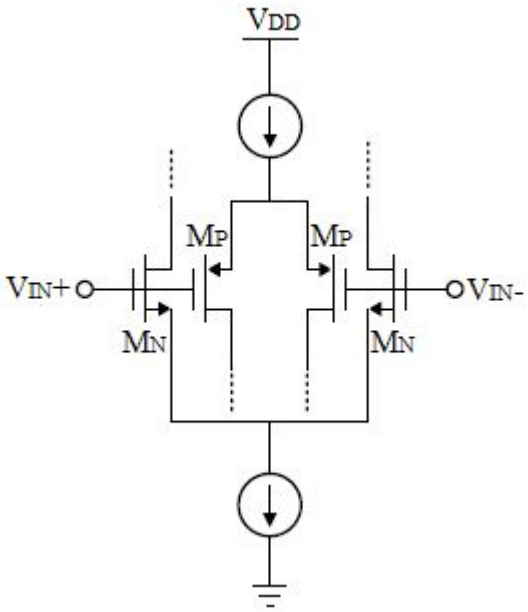

Fig.1: Rail-rail input-stage using complementary differential-pairs.

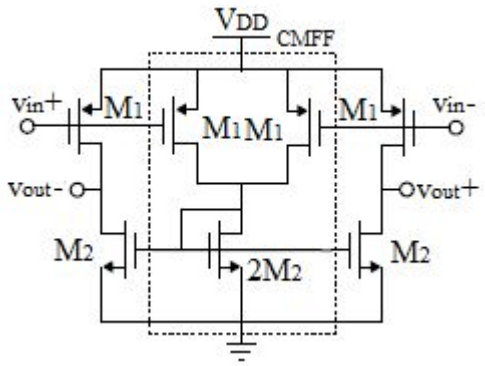

Fig.2: Pseudo differential pair with CMFF.

B. Bulk-Driven MOS Transistor

Fig.3. Similar to conventional gate-driven MOS transistor, gate-source voltage of a bulk-driven MOS transistor is fixed, but slightly above threshold level and to create a conducting channel between sources and drain regions. The channel is modulated by the ac input signal applied to a bulk terminal instead of the gate terminal. The minimum input voltage not limited by the threshold voltage of the transistor.

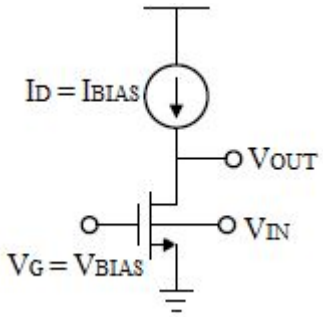

Fig.3: Bulk-driven NMOS transistor circuit operation.

III. PROPOSED BIASING TECHNIQUE

Operational Transconductance Amplifier (OTA), Differential input voltage produced an output current (VCCS), additional input for current to control.

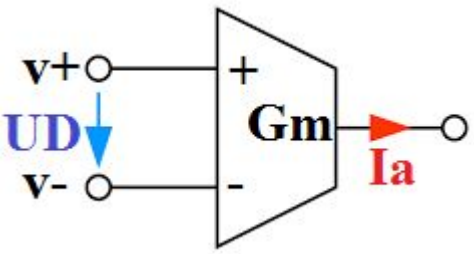

Fig.4: Symbol of OTA.

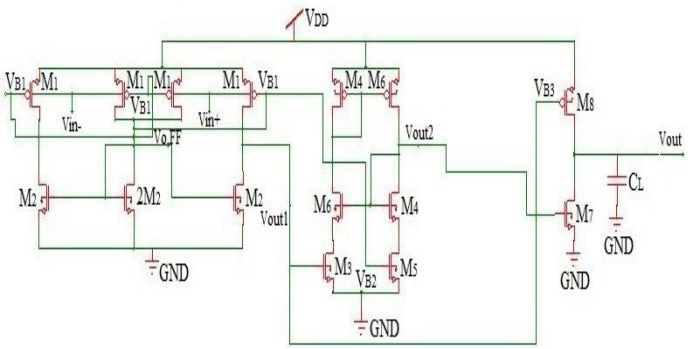

Fig.5: Open loop circuit OTA.

Fig.5. Open loop circuit operational transconductance amplifier can be design of voltage gain **56 dB** and phase margin 180-40 = 40. The circuit can be without damping factor network (DFC) design, and adding two transistor M_3 and M_5 in the second stage. First and third stage are

non-inverting stage and second stage are inverting common-mode stage.

$$A_{CM} = \frac{v_{out}}{v_{in,CM}} \simeq \left(\frac{g_{mb1}\, g_{m2}\, g_{m3}}{g_{m2}}\right)(r_{05} \parallel r_{06})(r_{07} \parallel r_{08})$$

Assuming the current-mirror transistor M4 and M6 same aspect-ratio, there realized same transconductance then differential gain **ADM** will be **(0) zero,** and common-mode gain **ACM** is found above equation and the corresponding common-mode rejection-ratio (CMRR) is

$$CMRR = \left|\frac{A_{DM}}{A_{CM}}\right| = \frac{1}{2} g_{m2}(r_{01} \parallel r_{02})$$

Close-loop operational transconductance amplifier can be performing of design unity gain frequency and power consumptions is reduce.

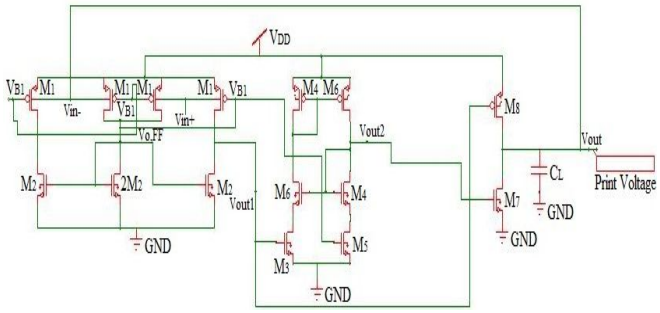

Fig.6: Close-loop circuit OTA.

Fig.6. Feedback work as a voltage follower, unity gain frequency is **1.16 MHz,** power consumption is **2.3738 µW**. Transistor M7 and M8 need are transconductance, which make suitable for low voltage application.

$$A_{DM} = \frac{v_{out}}{v_{in}} \simeq \frac{1}{2} g_{mb1}\, g_{m3} g_{m7}(r_{01} \parallel r_{02})(r_{05} \parallel r_{06})(r_{07} \parallel r_{08})$$

The differential-mode dc gain ADM proposed OTA can obtained from pole and zero of the circuit further analyzing the small-signal model.

IV. RESULTS AND SIMULATION

To confirm the validity of the claim made in this paper, The operational transconductance amplifier (OTA) circuits with self-biasing was fabricated in 65 nm CMOS technology. The operational transconductance amplifier (OTA) was design with a nominal dc gain **56 dB** and unity gain frequency **1.16 MHz** operating off a **0.5 V**.

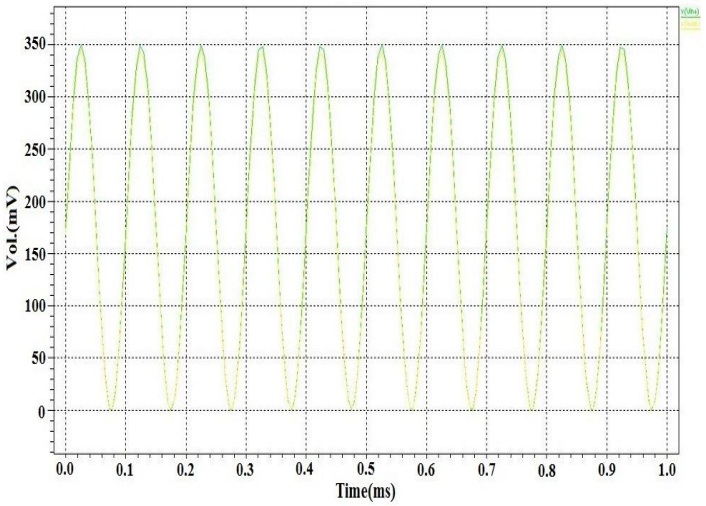

Fig.7: Unity gain frequency.

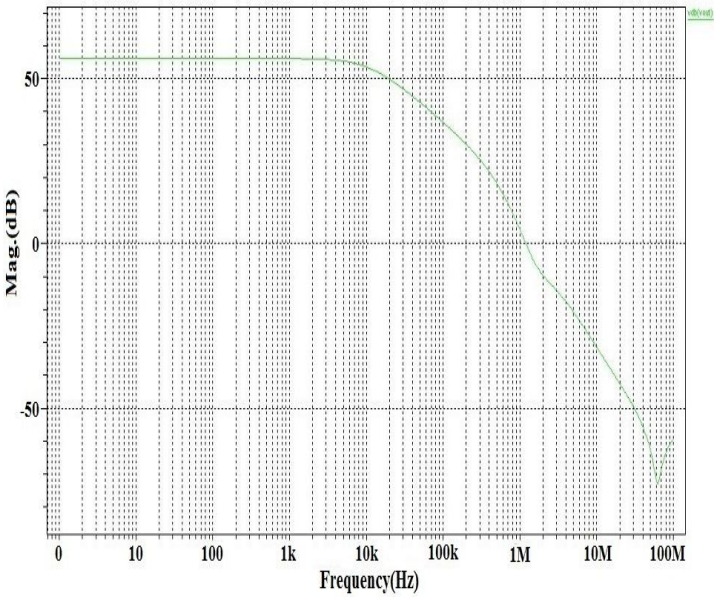

Fig.8: DC gain of OTA.

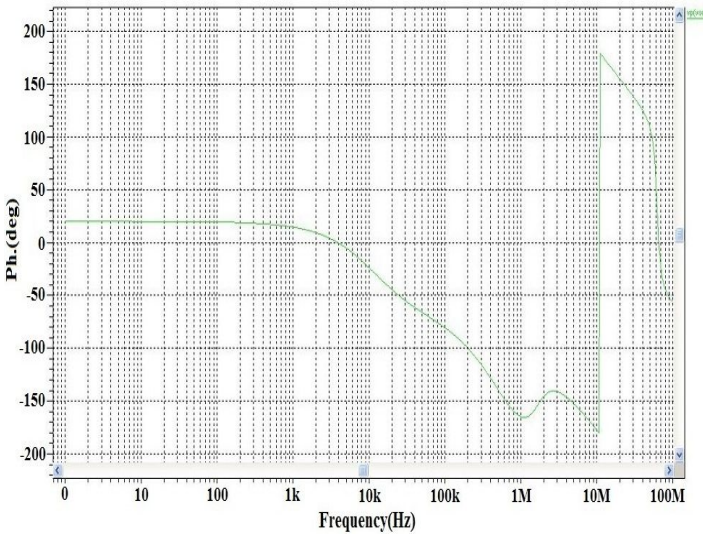

Fig.9: Phase-margin of OTA.

The transistor dimensions and operating conditions listed in Table I.

TABLE I
TRANSISTORS DIMENSIONS

Transistors	W	L
M_1	65 µm	160 nm
M_2	64 µm	160 nm
M_3	52 µm	160 nm
M_4	128 µm	160 nm
M_5	52 µm	160 nm
M_6	128 µm	160 nm
M_7	96.6 µm	160 nm
M_8	264 µm	160 nm

TABLE II
DESIGN PARAMETERS OF PROPOSED WORK

Parameters	Proposed work
Power Supply[V_{DD}]	0.5 V
Technology	65 nm
Software	Tanner

TABLE III
RESULT OF PROPOSED OTA

Parameters	Proposed OTA
Power	2.3738 µW
DC Gain	56 dB
Unity Gain Frequency	1.16 MHz
Phase margin	40

The Table 3. Provide all the detailed results of simulation done on tanner of the proposed circuit.

The Fig.6: tell about the power consumption of the proposed OTA which is **2.3738 µW**.

V. CONCLUSION

This paper presents OTA for ultra-low voltage operation was in modern CMOS technologies. The input stage of proposed OTA two low voltage techniques, first pseudo differential pair and bulk-driven MOS transistor. Proposed OTA simultaneously allow both minimum supply voltage operations and rail-to-rail input common-mode range. The proposed self-biasing techniques eliminate the need for extra biasing circuitry, allow saving area and power consumption. Three-stage OTA for low voltage application was design and fabricated in a **65 nm** CMOS technology.

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