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Design of Area, Speed and power Efficiency of different adders

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ABSTRACT: Area and speed are the most important aspects in integrated circuits. Since addition is the basic operation for all arithmetic computations, adders are the widely used components in all digital integrated circuit design. As propagation of carry is of major problem in designing efficient adders, this paper presents different fast adders and their performances are analyzed. When compared to all the adders, Square root Carry Select Adder (SQCSA) provides a good performance and low cost. SQCSA is still area consuming due to dual Ripple Carry Adder (RCA) structures, simple and efficient gate level modifications should be done to reduce area. Modified SQCSA is designed in such a way that it uses fast adders like RCA, Carry Look-Ahead Adder (CLA) and CSLA to increase the operation speed. Conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA are analyzed to study the data dependence and to identify redundant logic operations.

Key Words: Fast adders, Carry Select Adder (CSA), Modified Carry Select Adder (MCSA), Carry Look-Ahead Adder (CLA).SQCSA, Modified SQCSA.

1. INTRODUCTION

Low power, area efficient and high performance VLSI system are used in mobile devices, wireless receivers, and biomedical instrumentation. Adder is one of the key in hardware blocks in Arithmetic and logic unit and digital signal processing systems. The DSP applications where an adder plays a major role include convolution, digital filtering like in Discrete Fourier transform and Fast Fourier Transform, digital Communications and spectrum analysis. The performance of an adder is purely depends on the power Consumption during addition Operation. In rapidly growing electronic production, quicker units are not only of anxiety for design but also smaller area and less power become major concern for design of the VLSI circuits. So a VLSI designer has to optimize area, power and delay constraint for rising portability and Battery life of devices. As we know millions of instructions per second are performed in microprocessors. Speed of operation is the most significant constraint to be measured while designing multipliers. But it is difficult to achieve. So depending on application compromise between constraints has to be made. There are many ways to design adders.

II.RIPPLE CARRY ADDER

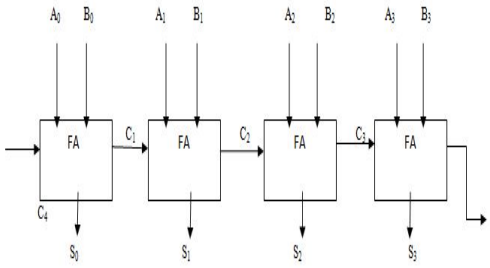

Figure 1. Block Diagram of Ripple Carry Adder:

Ripple carry adder is constructed using full adders. It is called a ripple carry adder since each carry bit gets ripple keen on the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occur. Transmission delays inside the logic circuitry are the reason at the back. The carry propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. It is one of the compact designs. But its speed of execution decreases as the number of bits increases. This is the main Disadvantage of this adder. Therefore we go for carry look ahead adder. Whereas carry look-ahead is the best ever but consume extra area. Carry select adders act as a conciliation between these two adders. A new concept of hybrid adders is presented in this paper to speed up addition process.

III.CARRY LOOK AHEAD ADDER

Improving the speed of addition will improve the speed of all other arithmetic operations. For that reason, dropping the carry propagation delay of adders is of immense importance. Different logic design approaches have been employed to overcome the carry propagation

problem. One of the method of speeding up this process by eliminating inter stage delay is look ahead carry addition. The adder circuit which does this operation is called as carry look-ahead adder. The fast method of adding numbers is called carry-look ahead. In this method the carry signal doesn't propagate stage by stage, instead it uses additional logic to expedite the propagation and generation of carry in order, allowing fast addition at the outlay of extra hardware. The logic for the generate (g) and propagate (p) values are given below.

$$Si=Pi\oplus Ci$$

$$Ci+1=Gi \oplus Pi\ Ci$$

Where, Pi is carry propagate and Ci is carry generate.

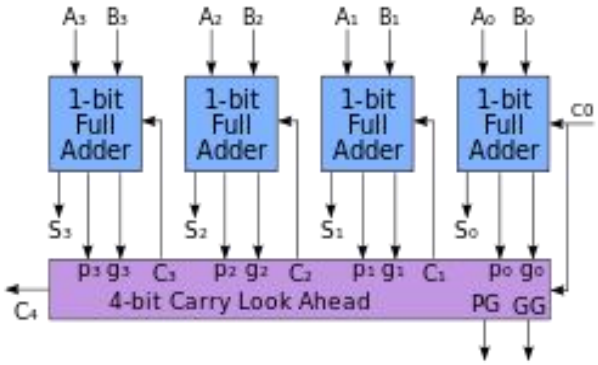

Figure 2. Block Diagram of Carry Look-Ahead Adder:

Look ahead carry generators can be cascaded to increases the word size in the multiples of 4-bits.Though the carry look ahead adder eliminates the propagation delay, the area consumption is more. Carry select adder acts as the comprise between these two adders(i.e) both speed and area efficient.

IV. CARRY SELECT ADDER

In electronics, a carry select adder is fastest adder used in many data processing operations. It uses dual RCA's to perform addition operation twice. One copy evaluates the carry by keeping the carry-in as '0',while the other computes by keeping carry-in as '1'.After the two results are calculated, the final sum and carry-out ,is selected with the MUX once the correct carry-in is known.

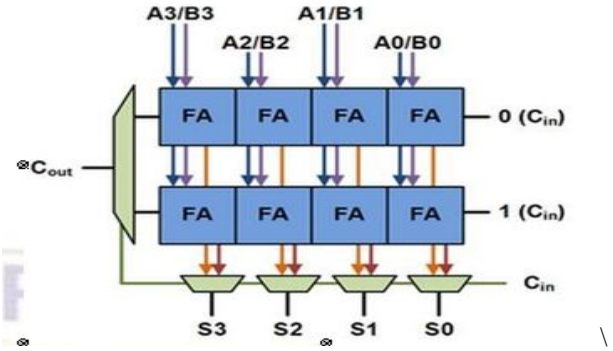

Figure 3. Block Diagram of Carry Select Adder

V. MODIFIED CARRY SELECT ADDER USING BEC

Here, the BEC unit is used along with RCA in order to reduce the area and power expenditure of the normal CSLA. To replace the n-bit RCA, an n+1-bit BEC is needed.

The Boolean expressions of the 4-bit BEC are given below:

X0=~B0
X1=B0^B1
X2=B2^(B0&B1)
X3=B3^(B0&B1&B2)

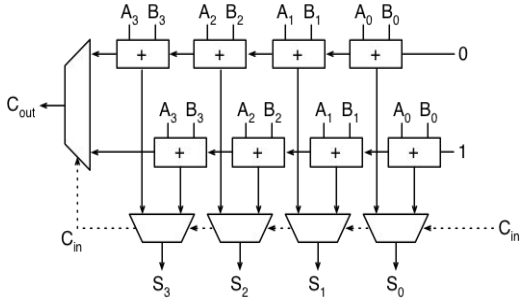

Figure 4. Block Diagram of Modified Carry Select Adder Using BEC

The basic function of CLSA is obtained by using 4 the MUX comes from RCA with cin=0 and another from BEC output. This produces two outputs mux select either BEC output or direct outputs according to the run signal .The significance of the BEC logic stem from the huge silicon area reduction when the CSLA with large number of bits are designed.

VI. SQUARE ROOT CARRY SELECT ADDER

The structure of the 16-b regular SQRT CSLA has five groups of different size RCA. The least significant bit stage is used to select the actual calculated values of the output carry and sum. One input to the multiplexer goes

commencing the RCA with Cin=0 and other input from the RCA with Cin=1. . The selection is done by MUX.

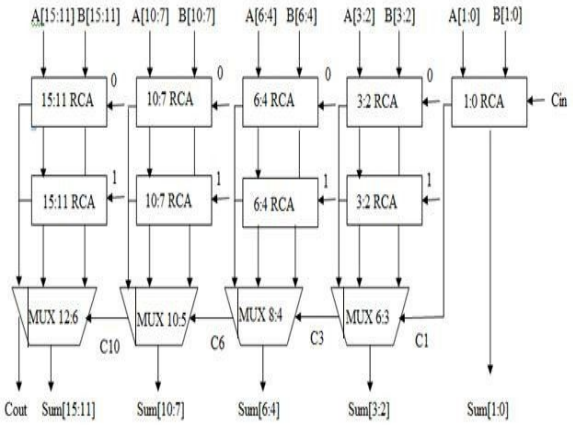

Figure 5. Block Diagram of Square Root Carry Select Adder

VII.MODIFIED SQRT CARRY SELECT ADDER

The modified sqrt-CSLA is obtained by replacing RCA by BEC.The structure of the projected 16-bit Square root CSLA using BEC for RCA with Cin=1 to optimize the power and area. Again split the structure into five groups. One input to the mux goes from the RCA with Cin=0 and other input from the BEC. On comparing the of both usual and modified CSLA, it is patent that BEC structure reduce the area and power. But the disadvantage of BEC method is that the delay is increasing than the regular CSLA.

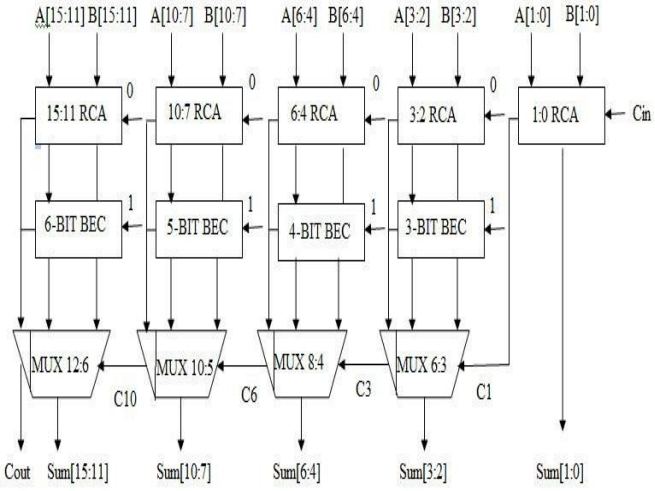

Figure 6: Block Diagram of 16-bit Modified SQRT with BEC.

Table 1 Comparison of Adder for Area, Delay and Power

Bit Size	Adder	Area(No. of Gate count)	Delay(ns)	Power (mW)
8 bit	RCA	210	13.98	96
	CLA	109	11.02	102
	CSLA	175	15.68	84.35
	square root CSLA	154	11.25	190.25
	Modified Square Root CSLA	108	12.87	147.35
16 bit	RCA	478	18.65	97.63
	CLA	265	14.58	158
	CSLA	398	20.14	80.32
	square root CSLA	352	15.12	302.1
	Modified Square Root CSLA	240	17.21	247.36
32 bit	RCA	1027	31.02	94.35
	CLA	542	25.06	302.85
	CSLA	847	34.01	77.35
	square root CSLA	781	24.02	541.31
	Modified Square Root CSLA	702	35.25	389.65
64 bit	RCA	2210	52.04	97.25
	CLA	1047	48.02	542.3
	CSLA	1874	55.35	75.4
	square root CSLA	1558	52.32	814.36
	Modified Square Root CSLA	1200	63.54	732.3

VIII.CONCLUSION

Area, Delay and Power are the element factors in VLSI design that confines the performance of any circuit. This effort presents a simple approach to reduce the area, delay and power of CSLA structural design. The usual carry select adder has the drawback of more power utilization and occupies more area. The proposed High Speed adders using common Boolean logic have low power, less delay and condensed area than all the other conventional adders. It is also little bit faster than all the other adders. In this way, the transistor count of High Speed adder is reduced. It has less area and low power which makes it simple and well-organized for VLSI hardware implementations.

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