

# Pre-Processing of ECG Signal using FPGA Implementation of DWT

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**Abstract** — In Bio-Medical engineering, ECG signal is used for the analysis of heart activity. For critical ECG is the electrocardiogram, the signal taken from the Heart to trace the activities. Digital Signal Processing (DSP) is the branch of Signal Processing which involves analysis/processing of signals eg ECG, EEG, EMG etc. This implementation DSP requires the FPGA with various algorithms, so for the pre-processing unit of ECG needs an embedded system based on FPGA. This design uses the Discrete Wavelet Transform (DWT) approach. Thus, the system deals mainly with the two Filters one Low Pass Filter & another High Pass Filter. As the DWT-based implementation requires important hardware architecture so our system is designed in such a way to reduce size, a FPGA consuming low power & size so it can be easily moved anywhere, a low cost as well. This whole system is designed by using Xilinx High-End Design Tools so it can be developed & simulated in proper as well as in easiest way. The Developed system is tested by using the ECG Signal from the database file from MATLAB. After the careful observation of the simulated results, it shows the system is giving proper response for suppression of BLW noise. JTAG Hardware co-simulation is used to test the BLW part from design. Xilinx SPARTAN 3 board which is having different diligent features is used to carry out the experiment. Typically this system is used in many Medical, Communication applications to remove noise from signal. Results comparison will be done on MATLAB.

**Index Terms** — FPGA, ECG, DSP, DWT, FPGA, Xilinx, MATLAB

## I. INTRODUCTION

The ECG (electrocardiogram) is the heart wave i.e. the signal taken from the heart to trace its activities. Those ECG Signals are used to diagnose the Heart Disorders. When taking this signal from heart it gets mixed with different other signals such as power-line interface, noise due to muscle activities, motion artifact etc. This may causes the addition of noise in the ECG Signal. ECG signal is taken from body by 6 different electrodes. Which works on the principle of potential difference on body surface generated by the heart electrical activity. This identification & extraction of ECG Signal reduces diagnostic accuracy. Therefore reduction of noise in ECG signal is the exclusive requirement.

Figure 1 illustrates the ECG Signal waveform, the ECG waveform is mainly composed of 5 different waves which reflect the activity of heart during a cardiac cycle (R-R interval). P, Q, R, S & T are the 5 different waves from heart. The Q, R, and S waves are called as QRS complex waveform and treated as a single composite wave describing the main heart activity.

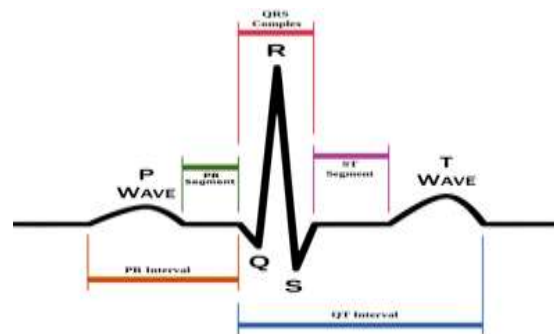


FIGURE 1  
ECG WAVEFORM INCLUDING ALL 5 WAVES

The ECG waveform from the heart shows when the heart contracts and relaxes and gives the heart rhythm of consecutive heartbeats. In a healthy heart the waveform pattern shows a regular shape and rhythm. In case of heart disease, abnormalities can be detected. The analysis of any ECG signal involves 3 stages: preprocessing stage for providing a "Noiseless" ECG, the extraction of the ECG signal should be proper for the diagnosis by the Expert. The aim of using pre-processing stage is to reduce the noise while the extraction of the ECG Signal. From these noises, the AC power line interference as well as the BLW produced by movements of patient and respiration are not easy to remove. In the ECG analysis, the QRS detection is a particular and separate operation.

## II. H/W AND S/W SYSTEM DESIGN

### A. Hardware

- Spartan-3 FPGA
- USB to Serial Converter

### B. Software

- Xilinx ISE
- Eclipse
- MATLAB

## III. PROPOSED SYSTEM

In the proposed system many operations are helping to get results. The steps which are following in block diagram are very crucial. We have designed the FPGA based embedded system for the ECG Signal Analysis which deals with the two different type of noise removal. One is BLW removal & another is QRS detection. As these both technique

requires the same type of signal processing we can use the same Hardware, which will in turn save the time, extra hardware requirements.

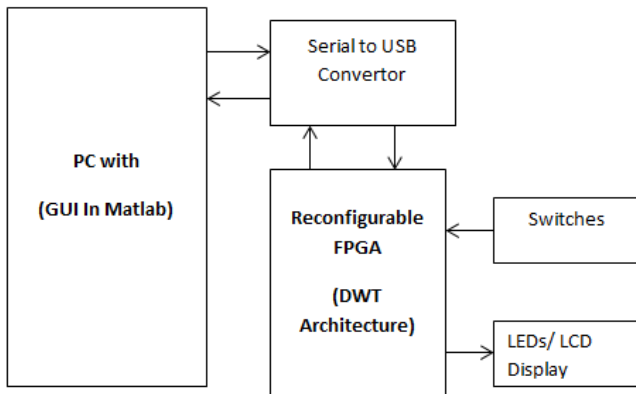


FIGURE2  
SYSTEM ARCHITECTURE

A. BLW Removal

BLW affects the ECG signal in major percentage so removal of BLW is the important factor. It is usually 0.8 Hzs hence it overlaps the ECG Signal & affects it badly. There are different approaches/techniques to remove this BLW noise. One approach is that by using the High Pass Filter which will remove all the high frequency component. It might add some delay in the ECG signal because of the time required by the filter to process the signal.

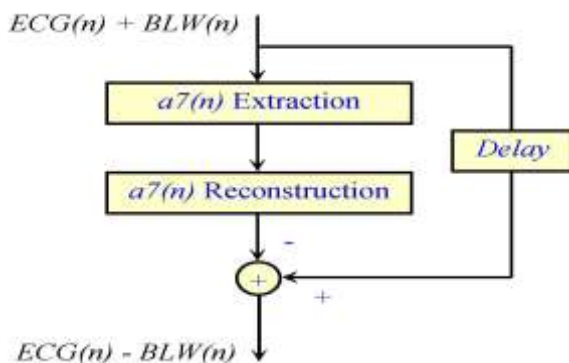


FIGURE3  
BLW NOISE REMOVAL

B. QRS Detection

The QRS Complex is the part of ECG wave which shows the major working of Heart. This ECG Signal can be seen on display. It is usually the central & most visually obvious part of tracing, It corresponds to depolarisation of left & right ventricles of Human Heart. To remove the noise form QRS detection we use Adaptive filter which will take decisions according to the input stage.

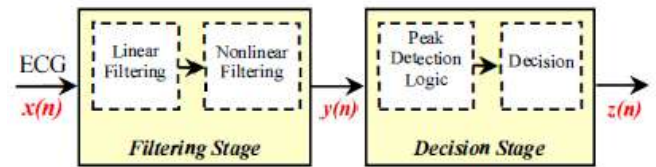


FIGURE4  
QRS DETECTION NOISE REMOVAL

IV. IMPLEMENTATION

A. Algorithm

1. Start
2. Loading ECG signal for Database
- or
3. Get file from User
4. Converting Signal samples in binary stream
5. Transmit Binary Data on Serial Port
6. Receive Data on FPGA by serial protocol
7. Decomposing input signal into low pass and high pass coefficients on fpga
8. Visualize decomposed output.
9. Retransmitting preprocessed ECG signal PC
10. Visualizing preprocessed ECG signal on PC
11. Calculating parameters like
  - PSNR
  - MSE
12. Stop

V. RESULTS

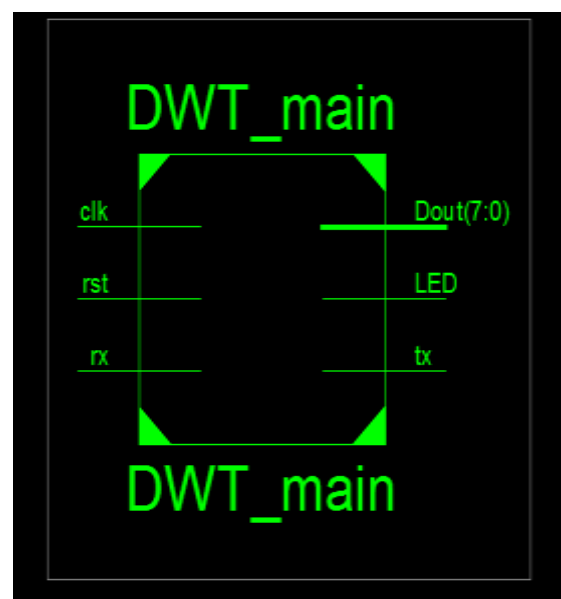


FIGURE5  
RTL SCHEMATIC

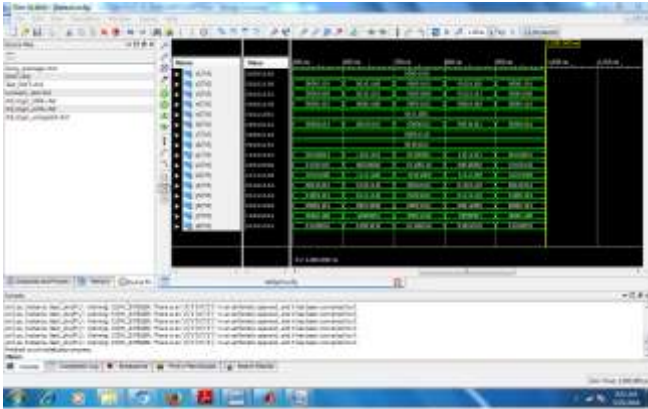


FIGURE6  
TESTBENCH WAVEFORM

TABLE 1  
DEVICE UTILIZATION SUMMARY

Parameter	Value (Out of)	Percentage (%)
No of Slices	55 / 704	7
No of Slice Flip Flops	55 / 1408	3
No of 4 input LUTs	106 / 1408	7
No of IOs	19	
No of bonded IOBs	19 / 108	17
No of GCLKs	2 / 24	8



FIGURE7  
ACTUAL SYSTEM IMPLEMENTATION

TABLE 2  
TIMING ANALYSIS SUMMARY

Parameter	Value
Minimum period	7.321ns (Maximum Frequency: 136.588MHz)
Minimum i/p arrival time before clock	5.212ns
Maximum o/p required time after clock	5.531ns
Maximum combinational path delay	5.900ns

VI. CONCLUSION

Different Noises get added to the ECG signal such as BLW Noise, inter-line interference etc. So we can use the technique of QRS detection & BLW Removal to remove most of the noise from the ECG Signal. The system simulation was successful resources constraint. Although, DSP system was developed on the DWT algorithm but it has responded in great way to get the output. If the more investigation/analysis is done on the same topic then it will definitely help to optimize the hardware implementations & delay in the circuit. We can make use of more software to simulate the same thing which is going to implement on hardware which will reduce mistakes/errors

VII. ACKNOWLEDGEMENT

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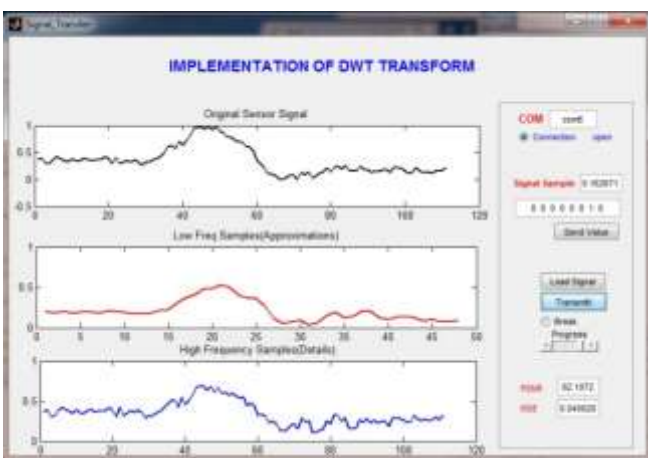


FIGURE8  
OUTPUT OF THE SYSTEM

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