ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 1, January 2017

DESIGN OF HIGH PERFORMANCE FIR FILTERS USING GDI TECHNIQUES

A.Gautami

Abstract— **A full adder is one of the most frequently used digital circuit component, many improvements have been made to refine the architecture of a full adder .In this paper 3 different types of full adders are compared with four different types of 10 transistors (10-T) GDI(gate diffusion input) full adders to test the performance of 7 adders .According to our test results, GDI full adders are better than the other CMOS logic designs which make it a better alternative. During this projected work the diffusion input theme is to decrease the ability in digital circuits. The system can provides the thought of low power logic style that may use reduced style space, less variety of devices and therefore the tiny power consumption. The projected system are enforced in Active TANNER machine.**

Keywords-component; GDI; CMOS; FULL ADDERS.

I. INTRODUCTION

A GDI full adders measure important structure blocks for varied digital signal processing (DSP) applications. Newly, thanks to the rising demand for video-signal process and broadcast, high-speed and high-order adders have been perform adaptative pulse shaping and signal leveling on the received information in real time, like ghost deletion, supply cryptography, and equalizer, Partial- Response most chance (PRML) and channel leveling. Signal dispensation algorithms usually want a substantial quantity of floating-point (or fixed-point) computations to be performed at real- time or close to period of time speeds. Hence, associate economical VLSI structural style for a high-speed full adder is needed. However, the massive range of concerned multiplications results in excessive hardware quality and power usage.

IC engineer's square measure needed to boost the presentation of existing method modules in some aspects, primarily in power reduction and size. Since the battery ability obtainable doesn't advance at identical rate because the electronics technology, IC designers have encountered additional constraints: high speed, high out turn, little element space, and at identical time, low power dissipation. Hence, the investigate of creating low power, high presentation adder cells is turning into feverish. One economical technique is to accomplish this task comes from the structural level. This approach is to coming up with associated analyzing an adder cell is moldering it into smaller modules for additional analysis and development. During this method, associate optimized full adder cell are often made by connecting these increased smaller modules. These square measures 3 basic approaches to decrease power consumptions of circuits in scaled technologies: reducing the spirited power consumption throughout the active mode method of the device and therefore the decrease of outpouring current throughout the stand-by mode.

II. GDI TECHNIQUES

A. Modified GDI Technique - A Power Efficient Method For Digital Circuit Design

In this system associated degree approach is gettable for minimizing power expenditure for digital circuits at the logic vogue level and DC and Transient analysis of basic logic gates has been done mistreatment Mod-GDI logic vogue. All Simulations square measure performed through PSPICE supported zero.18µm CMOS technology, and results show power characteristics of GDI technique of low power digital circuit style. Simulation results shows up to forty fifth reductions in power-delay product in Mod-GDI. Mod-GDI approach permits realization of a broad style of many-sided logic functions by means that of solely 2 transistors.

Mod-GDI gates lesser than the semiconductor count and successively the semiconducting material space needed when it put next to the traditional static CMOS and Domino CMOS primarily based approaches.

B. 16-bit Low Power Booth Encoded number style mistreatment GDI CMOS Logic Logic

This method offers an obvious plan of various number and planning a 16-bit number employing a technology referred to as GDI (Gate Diffusion Input). The aim of the number style in GDI is to indicate decrease of space within the number style compared to CMOS style. A relative study is complete regarding the full range of devices necessary for the number style mistreatment CMOS and GDI logics. It's determined that number designed in GDI leads to nineteen.1 % decrease of devices, therefore minimizing the realm of number.

C. GDI Technique: A Power-Efficient methodology for Digital Circuit

A novel GDI methodology for low-power style was gettable. Comparisons with existing TG and N-PG techniques were dispensed, showing associate degree up to forty fifth decrease of power-delay product within the check kick in GDI over CMOS and vital enhancements in performance. GDI can enable high thickness of manufacture as currently a day's chip space is incredibly vital parameter. The GDI methodology permits use of a straightforward and economical style formula, supported the Claude Shannon growth. It makes GDI appropriate for synthesis and realization of combinatorial logic in real LSI chips, whereas employing a single-cell library. This proves to be an extra good thing about GDI over CMOS and PTL. Implementations of GDI circuits in SOI or twin-well CMOS processes square measure inevitable to produce additional power delay economical style, as a result of the employment of a whole cell library with reduced semiconductor count.

D. Asynchronous Gate Diffusion input (GDI) Circuits

A novel methodology for asynchronous circuits was bestowed. It's supported the two-transistor GDI (Gate Diffusion Input) cells. A spread of GDI circuits was compared to traditional CMOS implementations. 5 GDI C-elements were developed and compared with 5 CMOS circuits. GDI dynamic and SR-latch circuits out performed CMOS in space, power and speed, however bound CMOS circuits area unit favored once static C-elements area unit required. GDI performs higher beneath reduced provide voltage, associated provides an increased tolerance to hazards. A Bundled-Data controller circuit showed that, beneath bound circumstances, associate all-GDI circuit needed less space, ran quicker and consumed less power than the CMOS equivalent.

A study of two combinatory logic circuits (XOR gate and a full adder) disclosed, however, that a GDI CMOS hybrid combination provides the best circuit. However in cases of low power or low noise associate all-GDI circuit ought to be thought-about.

E. Design and Implementation of Full Adder Cell with the GDI Technique supported zero.18µm CMOS Technology

The aim of this work is to provide power decrease and speed increase within the full adder. During this operation the GDI methodology was introduced. By mistreatment techniques like size optimizing fully adder may decrease the facility consumption. As a result, the total adder works at the one hundred rate speed with zero.78 µw power consumption. These results were obtained with spice simulation from the extracted internet list of the layouts for traditional parameters, temperature and power provide at 5v.

F. .Design of Wallace multiplier using gdi based 10T fulladder

The performance of various full adders in different CMOS logic styles and in depth the advantages and limitations of each of them with respect to delay, power dissipation and PDP is presented. Hybrid adders are chosen for the extensive evaluation and a new low power and high performance hybrid full adder is designed in 90nm Technology. The adder cell is categorized into three modules. The modules are two XOR gates designed using 4 transistors in Gate Diffusion Input (GDI) technique and third module is carry block designed using GDI mux.
Hybrid full adder shows low power and minimum delay. Due to the minimum time delay, the adder improves the overall performance. The disadvantage of transmission gate logic is that it requires double the number of transistors of the standard pass-transistor logic or more to implement the same circuit.

G. Design of low power cmos logic circuits using gate diffusion input (gdi) technique

The 4×1 Multiplexer, 8×3 Encoder, BCD Counter and Mealy State Machine were implemented by using Pass Transistors (PT), Transmission Gate (TG) and Gate Diffusion Input (GDI) technique and then they were compared with each other for power dissipation. The Multiplexers and Encoders are combinational circuits and Counters and mealy machines are sequential circuits both of them are very important digital systems so power optimization should be done to those digital circuits. The main advantage with this state machine is used to reduce the number of states. The mealy machines are developed by using Pass Transistors, Transmission Gates and Gate Diffusion Input. There are two main disadvantages with pass transistor design;

- One is the threshold voltage across the single channel Pass Transistor, which results in reduced drive and slow operation.
- Other one was, full swing voltage at output is not possible.

H. A diffusion based low power consumption approach to construct 90nm full adder

The proposed work is in same direction to reduce the power consumption in the construction of 90nm full adder with cmos architecture. This paper presents the filtration approach for high performance and low power architecture generation. in this proposed work the diffusion input scheme is introduce to reduce the power in digital circuits. The system will gives the concept of low power logic design that will use reduced layout area, less number of devices and the low power consumption. The proposed system will be implemented in active hdl or in the modelsim simulator. The simulation will be presented in the form of waveforms. The work will be independent to the layout. The obvious advantages of small transistor number and special structures make them better alternatives for future uses. The major aim of using these newly designed xor gate is to reduce power consumption in cmos full adders. The large number of involved multiplications leads to excessive hardware complexity and power consumption.

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 1, January 2017

I. Carry Select Adder design based on 11t 1bit full adder

Low power using 11transistors full adders have been proposed. The main goal of the design is to improve the performance of existing csa design based on 10 transistor full adders. Here the proposed csa circuits have negligible area overhead, really improved power consumption and temperature sustainability in comparison with existing design. The performance parameters such as power, delay and area were analyzed by using dsch2 and micro wind 3.1 tools on 90 nm technology.bec logic comes from the lesser number of logic gates than the n-bit full adder (fa) structure bec logic is that when large amount of the bits are sent to csa for addition bec logic usage saves a very large amount of area as compared to rca which is used in the conventional csa.Some amount of degradation is seen but that can be acceptable for cascaded structures.

The basic GDI cell is shown in Figure.1. It is a replacement methodology for low power digital combinatory circuit style. This method reduces power consumption, propagation delay and space of digital circuits whereas to maintain low complexness of logic style. The most dissimilarity between the CMOS and GDI primarily based style is that the supply of the PMOS in an exceedingly GDI cell isn't connected to VDD and therefore the supply of the NMOS isn't connected to GND. This feature offers the GDI cell 2 extra input pins to be used that makes the GDI style additional versatile than CMOS.

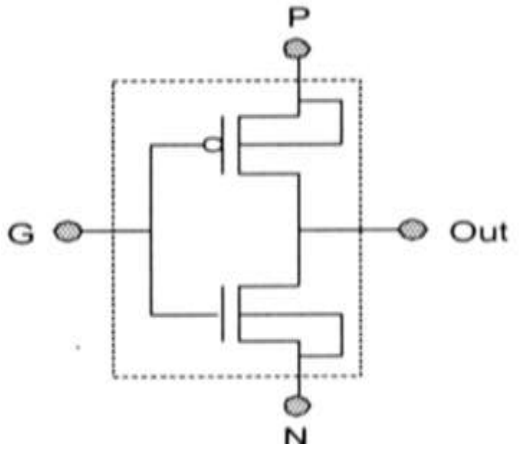


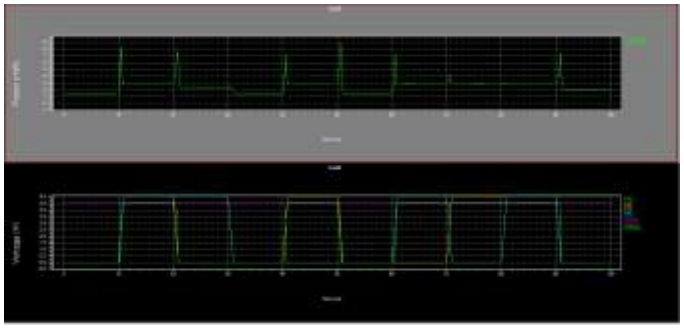
Figure.1 The basic GDI cell

GDI cell consists of 3 inputs - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of each nMOS and PMOS area unit connected to N and P severally. thus by mistreatment GDI methodology we will implement numerous logic functions with less power and high speed as compared to standard CMOS style.

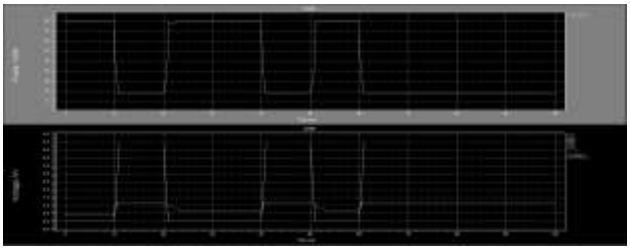
III.COMPARISON TABLE FOR FULL ADDERS

TITLE	POWER (watts)	DELAY (sec)	PDP
28CMOS	2.485e-003	2.00	0.24744
Transmission gate	3.506e-002	1.71	0.81137
14 T	1.412e-003	1.81	0.13145
GDI-xor1	2.742e-003	1.32	0.18020
GDI-Xnor1	8.529e-004	1.40	0.21869
GDI-Xor2	2.745e-003	1.31	0.17903
GDI-xnor2	8.574e-004	1.93	0.30308

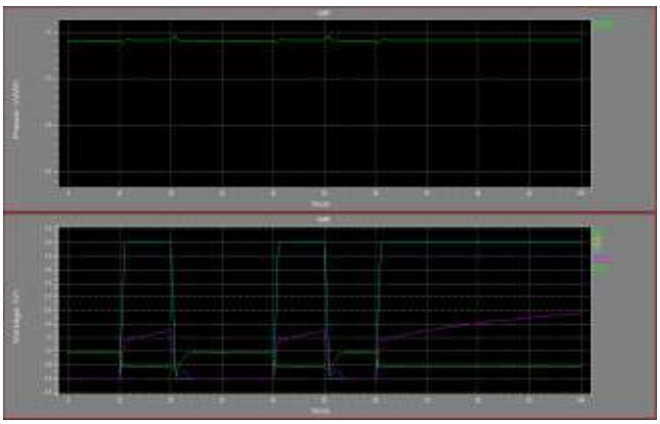
IV.WAVEFORMS FOR FULLADDERS



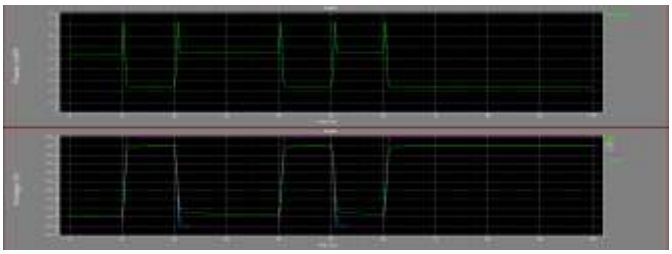
(a) *28-T*



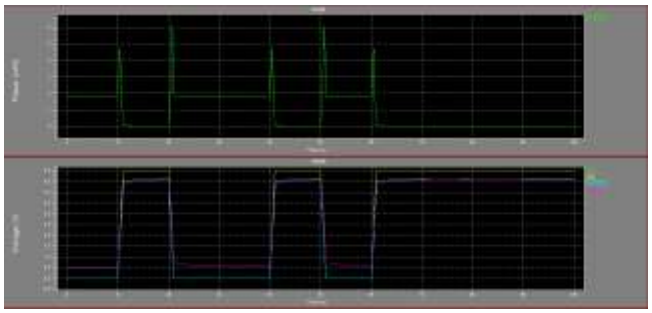
(b) *transmission gate*



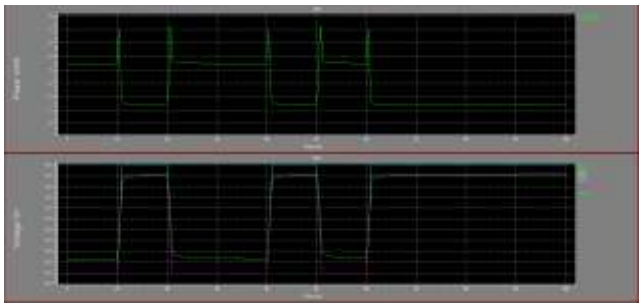
(c) *14-T*



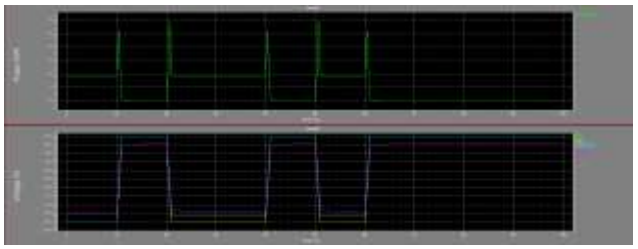
(d) *GDI xor1*



(e) *GDI xnor1*



(f) *GDI xor2*



(g) *GDI xnor2*

Figure:(a)28-T, (b), (c), (d),

V.CONCLUSION

In this paper, available low-power realizations of full adders are planned. Using this fulladder the efficient FIR filter is designed. The freshly designed modules possess the deserves of low power dissipation, and space saving thanks to lower junction transistor counts and special styles. Completely different blocks were designed victimization GDI technique specifically XOR computer circuit, Full Adder. The blocks were designed additionally, victimization of typical

Complementary Metal compound Semi-Conductor (CMOS) logic

REFERENCES

[1] J.M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits", 2nd edition, Prentice Hall, 2002,pp 491-621.

[2] N. Weste and K. Eshraghian, Principles of CMOS digital design. Reading, MA: Addison-Wesley, pp. 304–307.

[3] Morgenshtein, A. Fish, I.A. Wagner, "Gate-Diffusion Input (GDI) A Novel Power Efficient Method for Digital Circuits: A Detailed Methodology", Proc. of 14th IEEE International ASIC/SOC Conference, pp. 39-43, USA, Sept. 2001.

[4] Padmanabhan Balasubramanian and Johince John" Low Power Digital Design Using Modified GDI Method" IEEE 2006,pp 190193.

[5] Morgenshtein, A. Fish, I.A. Wagner, "Gate-Diffusion Input (GDI) A Technique for Low Power Design of Digital Circuits: Analysis and Characterization", Proc. of ISCAS"02 Conference, vol. 1, pp. 477-480, USA, May 2002.

[6] Morgenshtein, A. Fish, I.A. Wagner, "Gate-Diffusion Input (GDI) A Power Efficient Method for Digital Combinatorial Circuits", IEEE Transactions on Very Large Scale Integration Systems, vol. 10, no. 5, pp. 566-581, October 2002.

[7] Morgenshtein, A. Fish, I.A. Wagner, "GDI (Gate Diffusion Input) Circuits for Fast and Low-Power Implementations of Logical Gates", US Patent Application no 60/406,751, 2003.

[8] Morgenshtein, M. Moreinis and R. Ginosar, "Asynchronous GateDiffusion-Input (GDI) Circuits", IEEE Transactions on Very Large Scale Integration Systems, vol. 12, no. 8, pp. 847- 856, August 2004.

[9] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low power 10-transistor full adders using novel XOR-XNOR gates,"IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol.49, no. 1, pp. 25–30, Jan. 2002.

[10] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage swing nodes," in Proc. IEEE Workshop Signal Processing Systems, Oct. 1999, pp. 713–722.

Ms. A. Gautami completed P.G in ECE from SNS college of Technology,Coimbatore in 2013, Working as Assistant Professor, ECE Department SNS College of Technology, Coimbatore. Fields of Interest are Wireless Sensor Networks and Digital Electronics