

# Analysis and design of a low voltage low power lecturer inverter based double tail comparator

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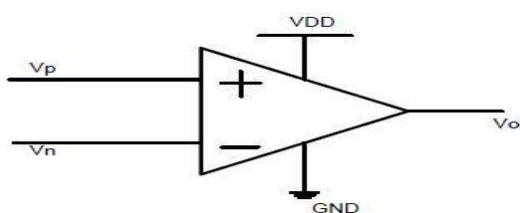
**Abstract:** Another outline of comparator which is primary piece of ADC is proposed. In this paper new plan of twofold tail comparator with cutting edge system of regenerative inverter is present. Proposed inverter gives less power scattering less postponement than traditional inverter. New proposed plan gives 25% decrease in power diminishment and 75% lessening in kickback clamor which is most essential parameter of comparator. The new outline is recreated in TSMC180nm in Tanner device which are measured to decide control scattering, speed and kickback clamor. These are contrasted and past outlines.

**Index Terms—** Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design.

## Introduction

The schematic symbol and basic operation of a voltage comparator are shown in fig.1 the comparator can be thought of as a decision making circuit.

Definition:-



The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the  $+V_p$  the input of the comparator is at a higher potential than the  $V_n$  input, the output of the comparator is a logic 1, where as if the  $+V_p$  input is at a potential lower than the  $-V_n$  input, the output of the comparator is at logic 0.

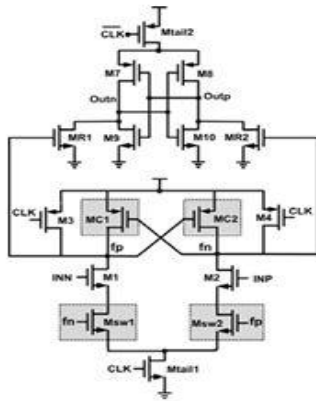
$V_P < V_N$  then  $V_O = V_{SS} = \text{logic } 0$ .

$V_P > V_N$  then  $V_O = V_{DD} = \text{logic } 1$ .

Comparator is basic building block of analog ADC circuit which is used to compare tow voltage level and gives output in digital form. The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative and the pros and cons of structure is discussed. The proposed comparator is presented in Section III. Section IV Simulation results are addressed in Section. Followed by conclusions in Section V.

## CLOCKED REGENERATIVE COMPARATOR

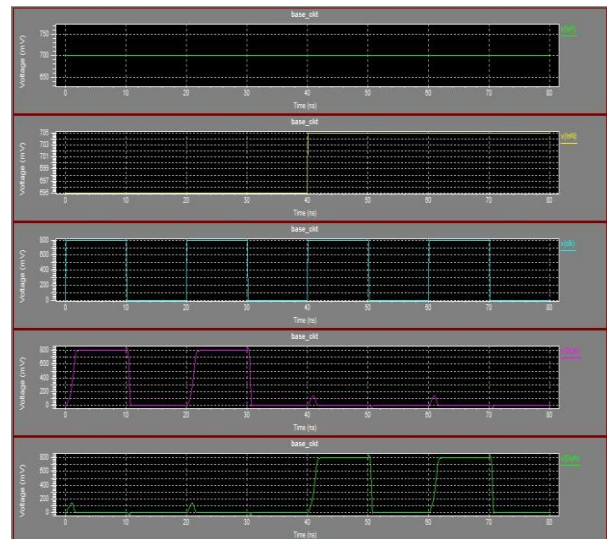
### 1. Conventional Double-Tail Dynamic Comparator



**Fig. 3 Schematic Diagram of the Dynamic Comparator**

Fig. 3 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure.

## 2. Operation of the Double-Tail Dynamic Comparator



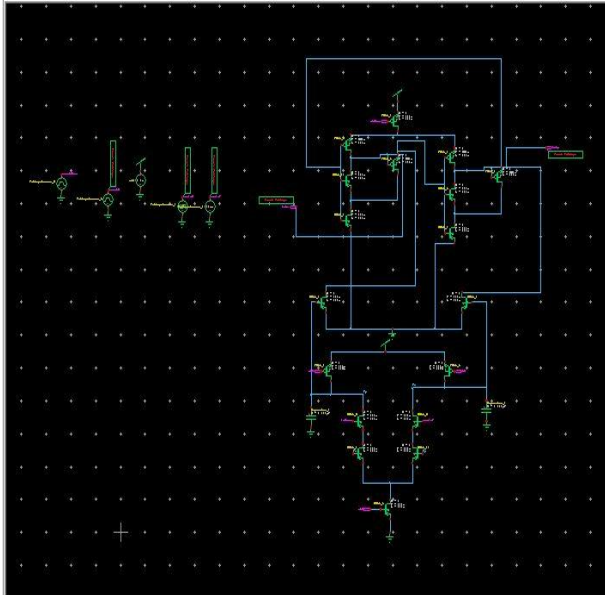
**Fig. 4 Transient simulations of the double-tail dynamic comparator for input voltage difference of  $V_{IN} = 5$  mV,  $V_{cm} = 0.7$  V, and  $V_{DD} = 0.8$  V**

The operation of the proposed comparator is as follows. During reset phase ( $CLK = 0$ ,  $nmos9$  and  $pmos1$  are off, avoiding static power),  $nmos2$  and  $nmos8$  pulls both  $fn$  and  $fp$  nodes to  $V_{DD}$ , hence transistor  $pmos3$  and  $pmos7$  are cut off. Intermediate stage transistors,  $pmos8$  and  $pmos5$ ; reset both latch outputs to ground.

During decision-making phase ( $CLK = V_{DD}$ ,  $nmos9$  and  $pmos1$  are on), transistors  $pmos8$  and  $pmos5$  turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since  $fn$  and  $fp$  are about  $V_{DD}$ ). Thus,  $fn$  and  $fp$  start to drop with different rates according to the input voltages. Suppose  $V_{INP} > V_{INN}$ , thus  $fn$  drops faster than  $fp$ . As long as  $fn$  continues falling, the corresponding pMOS control transistor starts to turn on, pulling  $fp$  node back to the  $V_{DD}$ ; so another control transistor remains off, allowing  $fn$  to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which  $V_{fn}/V_{fp}$  is just a function of input transistor transconductance and input voltage difference in the proposed structure as soon as the comparator detects that for instance node  $fn$  discharges faster, a pMOS transistor turns on, pulling the other node  $fp$  back to the  $V_{DD}$ . Therefore by the time passing, the difference between  $fn$  and  $fp$  ( $V_{fn}/V_{fp}$ ) increases in an exponential manner, leading to the reduction of latch

regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors turns on, a current from  $V_{DD}$  is drawn to the ground via input and tail transistor resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors.

### PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

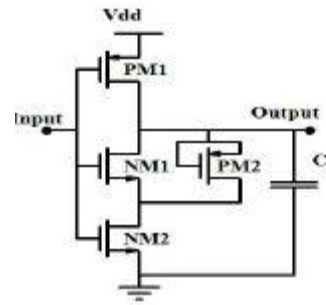


**Fig 5 Schematic diagram of the proposed dynamic comparator**

Operation of proposed is same as dynamic double-tail comparator. But for further reduction in parameter such as power delay pdp energy we analysis the circuit and replace regenerative inverter by new inverter.

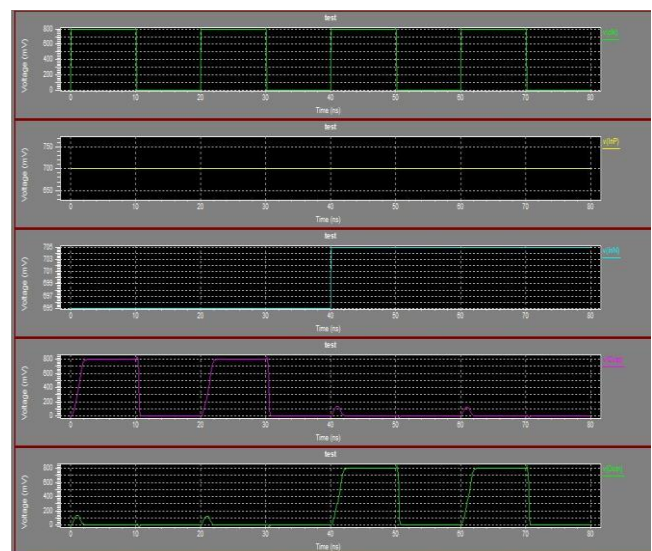
As we are moving to more and more scaling technology our size of transistor channel decreases by new proposed technology, due to which leakage power is reduces in circuit, as well as our circuit become more flexible in occurrence with parameter.

### Proposed Inverter



**Fig.6 Proposed Inverter**

We describe a new leakage power reduction technique called LECTOR (Leakage Control Transistor) for designing CMOS inverter circuits. In the proposed technique, we introduce two leakage control transistors (a p-type and a n-type) within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. In this arrangement, one of the LCTs is always “near its cutoff voltage” for any input combination.. The basic idea behind our proposed approach is to raise the voltage at the source terminal of the MOS transistor to reduce the leakage currents so as to minimize the static power dissipation. Considering these two facts, sub-threshold current can be minimized by reducing the drain to source voltage. Drain to source voltage can be reduced by raising the voltage at the source terminal of the MOSFET called source biasing.



**Fig7 Transient simulations of the proposed double-tail dynamic comparator for input voltage difference of  $V_{IN} = 5$  mV,  $V_{cm} = 0.7$  V, and  $V_{DD} = 0.8$  V.**

## REFERENCES

PARAMETERS	BASED PAPER DOUBLE TAIL COMPERATOR	NEW DOUBLE-TAILCOMPARATOR(LECTOR INVERTER)
TECHNOLOGY	180nm	180nm
APPLIED VOLTAGE	0.8v	0.8v
POWER(nw)	904.58	706.22
DELAY(output)(ns)	1.1577	1.2101
DELAY( outn)(ns)	1.1280	1.1834
PDP( outp) (fJ)	1.0472	0.8546
PDP( outpn) (fJ)	1.204	0.8357
ENERGY(fJ)	72.36	56.49
KICKBACK NOISE(MV)	14	4

## SIMULATION RESULTS

In order to compare the proposed comparator with the conventional and double-tail dynamic comparators, all circuits have been simulated in a 0.18- $\mu\text{m}$  CMOS technology with  $V_{DD} = 0.8 \text{ V}$ .

## PERFORMANCE COMPARISON

## CONCLUSION

We studied different comparator which plays very important role in analog ADC circuit. Depending on that work we came on conclusion that there is scope of improvement in comparator circuit. Because present comparator is giving more power dissipation and also kickback noise is most important parameter concern. So, we define new double tail comparator with modified regenerative latch inverter with source biasing technique which gives source voltage in off stage which increases drain to source voltage giving reduction in leakage threshold current causing reduction in leakage power in output side which gives less power dissipation and most important reduction in kick back noise.

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