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Analysis of Reversible Gates with vedic concept on 4-bit Ripple Carry Adder Using Tanner EDA Tool

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***Abstract*— VLSI circuit design is the most emerging field technology. Now a days reversible logic gates is a vital issue for speed and zero power consumption. This paper is based on Vedic multiplier algorithm URDHVA TIRYAKBHYAM (UT) which is a most powerful multiplication. Urdhva Tiryakbhayam means vertically, crosswise and vertical crosswise multiplication is used. In this work we analysed the design of 4bit ripple carry adder using three HNG gates and ones PERES gate. HNG gates means haghparast navi gate. It is better than the existing counter parts in terms of no of gates, garbage output and constant input. PERES gate is a reversible logic gates which attracted a lot of attention due to zero power dissipation under ideal condition. Reversible logic circuits are useful for constructing quantum computers. Reversible logic using Vedic multiplier based on the urdhva Tiryakbhayam so that we can achieve the best result for delay, size, power and quantum cost. The main applications are DSP like imaging, wireless communication, software defined radios, filters. The proposed system is designed by the software using TANNER EDA version 15.0, 32 bit.**

***Keywords*—Reversible Logic Gates; urdhva tiryakbhayam; TannerEDA.**

I.INTRODUCTION

In modern VLSI circuit design, important goal is reduction of power dissipation. Arithmetic operation like multiplication is very important goal. It is one of the most silicon intensive functions, especially when implemented in Programmable Logic. Multiplier is the IMPORTANT key components of many high performance systems such as DSPs, Microprocessors and FIRs etc. The performance of systems is dependent on the performance of the multipliers because the multiplier is generally the slowest element in the system. Generally it is most area consuming. Hence optimization of speed and area of multiplier is a major design issue during the designing of the circuit.

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Vedic mathematics is the set of rules which deals with some mathematical formulae. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krishna Tirth [1]after his research on Vedas .He has invented 16 sutras. Urdhva Tiryakbhayam is one among them which is more efficient. Urdhva Tiryakbhayam is a Sanskrit word which means vertical and crosswise in English.

This paper is the extension of the previous work which tries to optimize the circuit proposed in the paper. It is organized as follows. Section two says about Literature survey, section third gives the basic knowledge of Reversible Logics. Section four explains the Urdhva Tiryakbhayam algorithm. Section five describes the modification of the previous design in order to evolve the optimized design. Section sixth brings the result obtained from reversible multipliers. Section seventh draws a conclusion which claims the versatility of this Reversible Urdhva Tiryakbhayam Vedic multiplier.

One of the solutions to meet the low-power requirement of the future devices is by adopting an entirely new model known as reversible logic in contrast to the existing irreversible logic. Reversible logic finds its origins in the concepts of Quantum Computing [18]. Researchers like Bennett showed that the devices based on reversible computing consume much less power than the traditional irreversible output vectors, thereby preventing loss of information, which in turn results prevents dissipation of energy, as shown by Landauer [5][6]. Different arithmetic circuits such as Adders, Subtractors, Multipliers, Carry Adders etc. based on reversible are available in literature. This paper focuses on the implementation of the Vedic multiplier in reversible logic.

The essential Vedic Mathematics lies in the fact that it is one of the most potent tools available to simplify extremely laborious mathematics [7]. Vedic mathematics is broadly used in reference to a series of 16 mathematical tricks that often make calculations simpler [7][8]. By reducing the number of steps involved, it greatly reduces computational time and at the same time improves accuracy. In this paper, the authors focus on the Vedic multipliers. These multipliers in contrast to the traditional multipliers like array multiplier, Booth multiplier, Wallace Tree multiplier etc., are area efficient, low power dissipating and exhibits high speed/low latency [9].

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II. REVERSIBLE LOGIC

A reversible logic gate is an n-input n-output logic device with one-to-one corresponding mapping. With the help of this logic gates the outputs are determine from the inputs and also the inputs can be uniquely recovered from the outputs. The fundamentals of reversible computing are based on the relationship between entropy and heat transfer between molecules in the system, the probability of a quantum particle occupying a particular state at any given time.

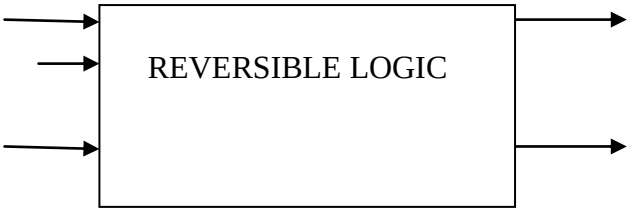

Figure 1:Reversible Logic

PARAMETERS:

A reversible circuit should be designed using minimum number of reversible logic gates. There are many parameters which are used for determining the complexity and performance of the circuits for designing a reversible circuit are:

a) ***Number of Reversible gates (N):*** The total number of reversible gates used in the circuit
b) ***Constant inputs (CI):*** It is defined as the numbers of inputs are to be maintained constant at either 1 or 0 in order to synthesize the given logical function.
c) ***Garbage outputs (GO***): It refers to the number of unused [4] outputs present in a reversible logic circuit. These are very essential to achieve reversibility so, it cannot be avoided.
d) **Quantum cost (QC):** It refers to the cost of the circuit in terms of the cost of a primitive gate.
e) ***Gate levels (GL)*:** This refers to the number of levels in the circuit which are required to realize the given logic functions

BASIC REVERSIBLE GATE:

PERES GATE: It is a 3x3 gate and its logic circuit is as shown in the figure.3 The quantum cost of this gate is four. It is used to realize various Boolean functions such as AND, XOR and outputs P = A; Q = A XOR B; R = AB XOR C.

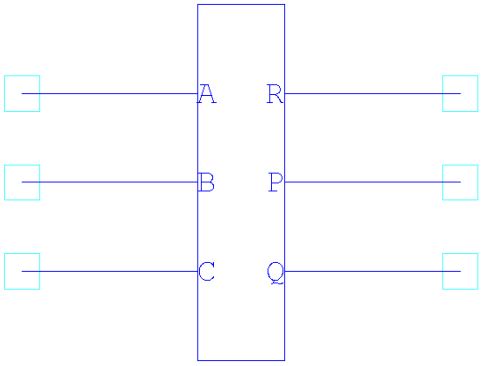

Figure 2: Peres Gate

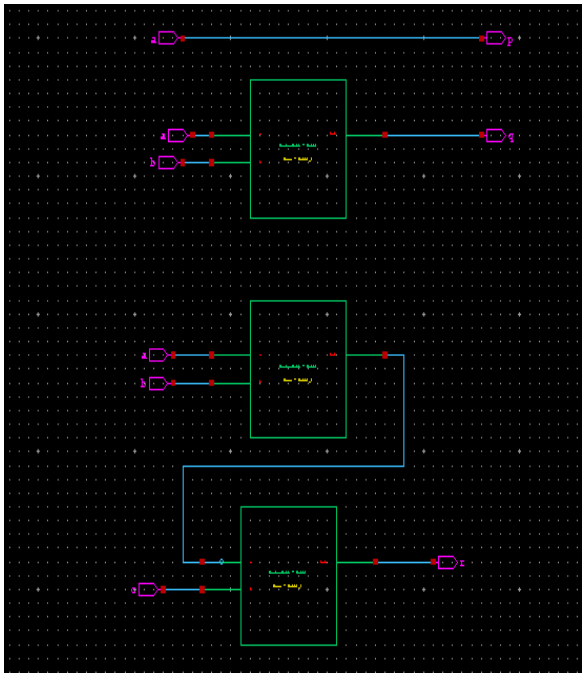

Figure 3: Interior structure of Peres Gate in Tanner

TRUTH TABLE FOR PERES GATE

INPUT			OUTPUT		
A	**B**	**C**	**P**	**Q**	**R**
0	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**	**1**
0	**1**	**0**	**0**	**1**	**0**
0	**1**	**1**	**0**	**1**	**1**
1	**0**	**0**	**1**	**1**	**0**
1	**0**	**1**	**1**	**1**	**1**
1	**1**	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**0**	**0**

FEYNMAN GATE: It is a 2×2 reversible gate .This gate is also known as Controlled Not (CNOT) gate. The Quantum cost of a Feynman gate is 1.This gate is generally used for Fan Out purpose. The inputs are (A, B) and outputs are P=A, Q= A XOR B.

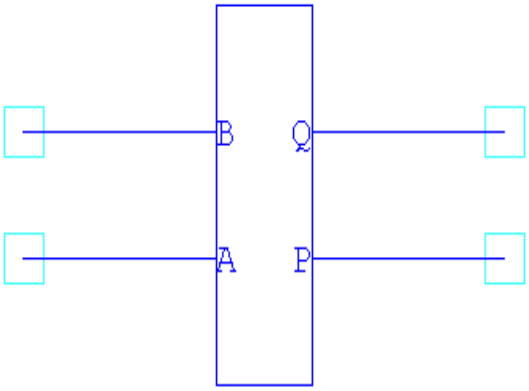

Figure 4: Feynman Gate

TRUTH TABLE FOR FEYNMAN GATE

INPUT		OUTPUT	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

HN GATE:

It is a 4x4 gate and its logic circuit is as shown in the below figure. The quantum cost of this gate is six. This gate is used to design a ripple carry adder. HNG [7] can produce both sum and carry in a single gate thus minimizes the garbage output and gate counts and the outputs are P = A, Q = B, R = A XOR B XOR C, S = (A XOR B)C XOR AB XOR D.

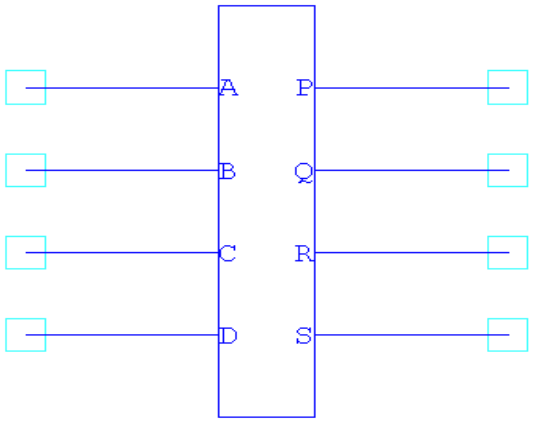

Figure 5: HNG Gate

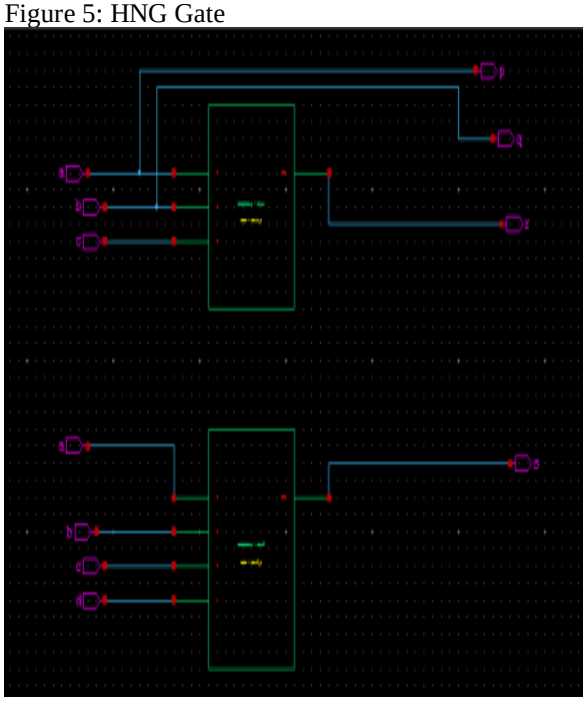

Figure 6: Interior structure of HN Gate in Tanner

TRUTH TABLE FOR HN GATE:

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

III. TANNER EDA SOFTWARE

Tanner EDA provides a complete line of software solutions that catalyze innovation for the design, layout and verification of Analog and Mixed Signal (A/MS) integrated circuits (ICs). Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RF devices.

In this Software, the circuits are designed in S-Edit Schematic Capture. Tanner S-Edit Schematic Capture increases the design productivity while handling the most complex IC designs. This powerful environment supports fast and cross-probing between schematic, layout and LVS reporting at net and device levels. Tanner Waveform Viewer (formerly known as W-Edit) provides an intuitive multiple-window, multiple-chart interface for easy viewing of waveforms and data in highly configurable formats.

IV. MULTIPLICATION ALGORITHM OF URDHVA TIRYAKBHAYAM

'Urdhva –Tiryakbhayam is one of the 16 sutras which is applicable to all cases of multiplication such as Binary, Decimals and Hexadecimals. It means vertically and crosswise. It works on the basis of novel concept of all the partial products generated and then additions of these partial products are performed concurrently. The partial products generated in parallel and their summation is obtained using this formula. In other multipliers with increase in the number bits of multiplicand or /and multiplier the time delay in computation of the product increases proportionally but this

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multiplier does not increases proportionately. Due to this fact time of computation is independent of clock frequencies of processors. Hence the clock frequency can be limited to a lower value. Since processor which uses lower clock frequency dissipate lower energy and it is economical in terms of power factor to use low frequency processors employing the fast algorithms. So by using Urdhva Tiryakbhayam Sutra in binary multiplication, the number of steps required to calculate the final product is reduced so computational time is reduced and increases the speed of the multipliers.

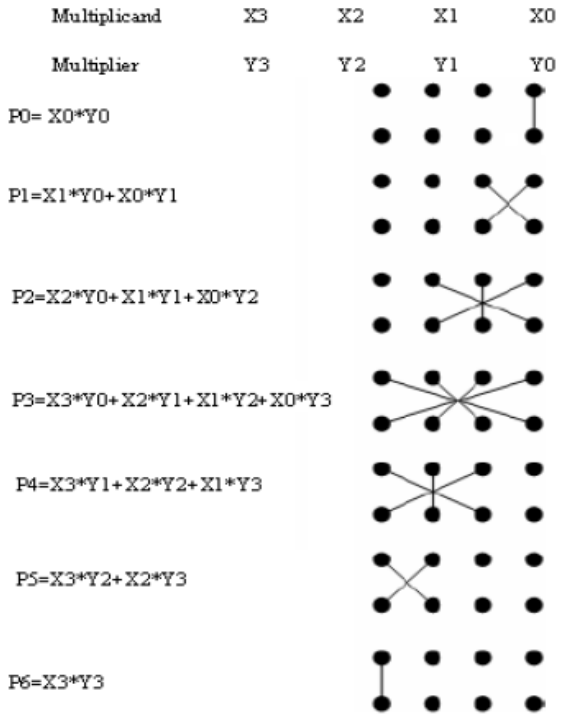

Figure 7: Multiplication procedure for 4X4 bit using 'Urdhva-Tiryakbhayam' sutra

Optimization and Hardware Implementation of Urdhva Multiplier:

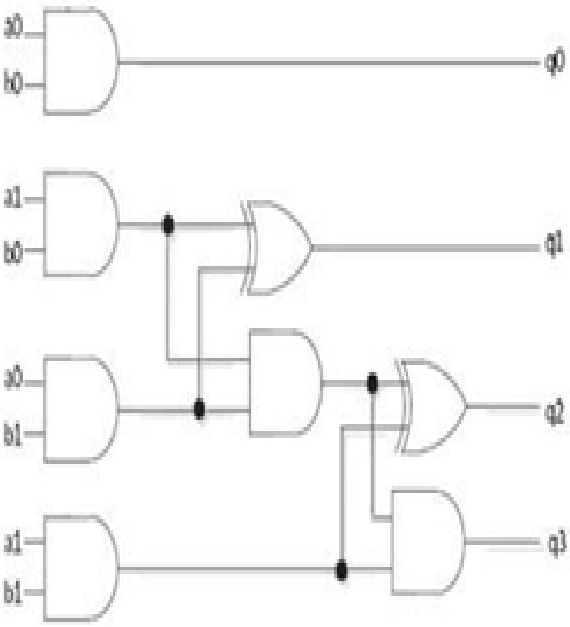

Figure 8: 2X2 UT Multiplier Using Reversible Logic Gate

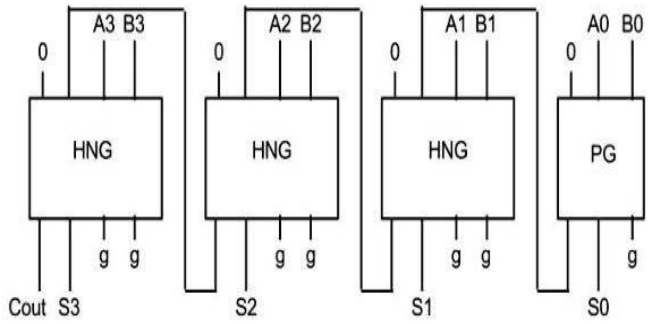

Figure 9: 4 bit ripple carry adder design

Block diagram of 4x4 is shown in Fig. 6. In this block four 2x2 multipliers are arranged systematically. Each multiplier accepts four input bits; two bits from multiplicand and other two bits from multiplier. Addition of partial products are done using two four bit ripple carry adder and 5bit rca .

V.EXPERIMENTAL RESULT ANDLAYOUT

The basic reversible gates such as Peres, HNG and XOR are designed and these circuits are used to design the 4 Bit Ripple Carry Adder, which are simulated using "TANNER EDA Software". Table 1 discuss about the comparison of the some important parameters of Reversible gates.

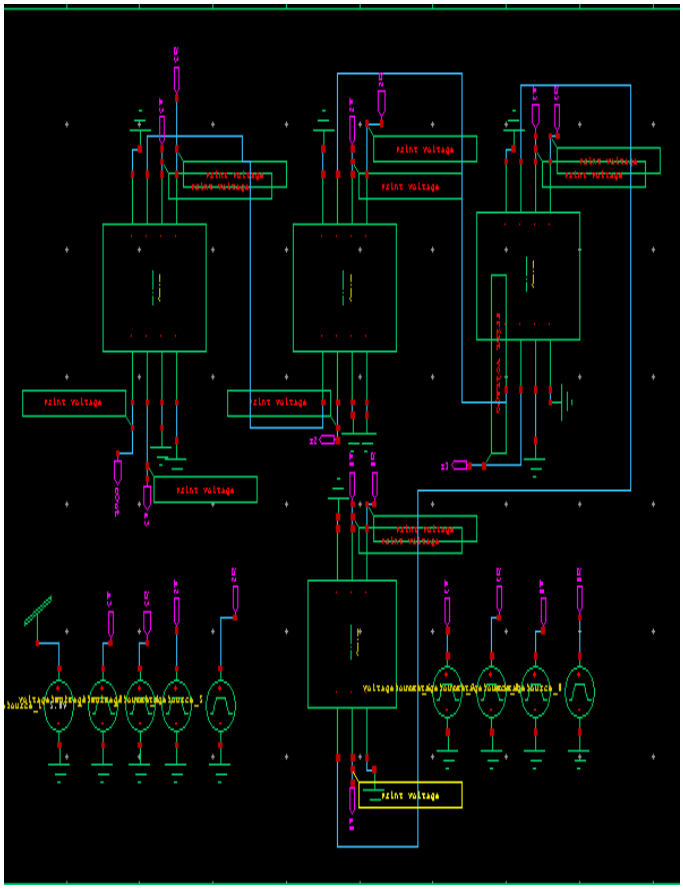

Figure 10: Implementation of 4 Bit Ripple Carry Adder

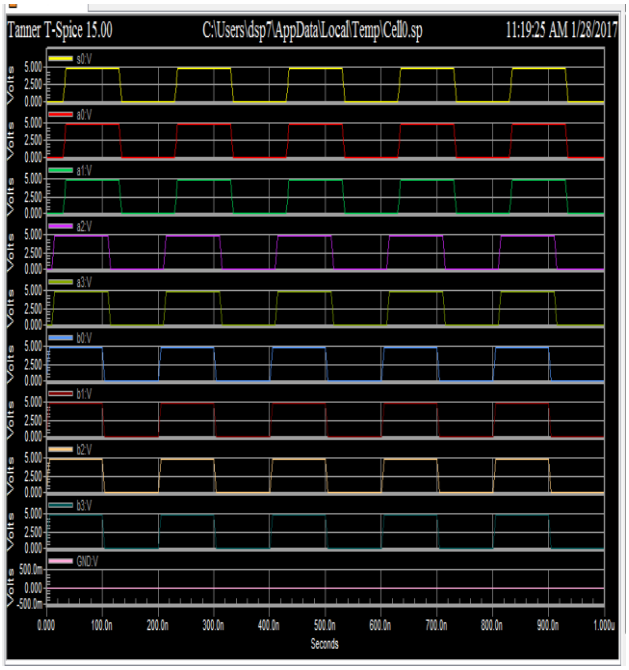

Figure 11: Simulation Result for 4 Bit Ripple Carry Adder

Reversible Multiplier	Number of Gates N	Number of Constant Inputs	Number of Garbage Outputs
Proposed (FG,PG,HNG)	28	28	60
[3]	40	31	56
[4]	29	34	56

The Layout of each gates are used to design the Integrated Circuit of Reversible Gates. L-Edit are used to generate the layout of 4 Bit Ripple Carry Adder using 2x2 UT Multiplier which is shown in below.

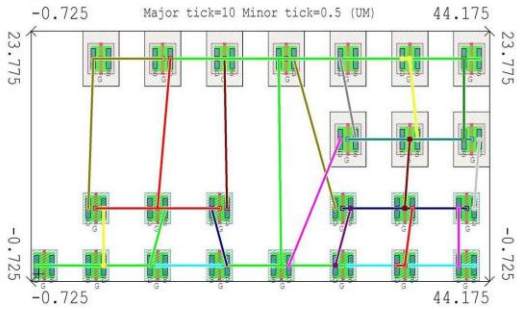

Figure 12: Layout of 4 Bit Ripple Carry Adder

VII. CONCLUSION

In this paper we concentrated on designing the 4 Bit Ripple Carry Adder using TANNER. By using reversible gates we can reduce the power dissipation. The proposed Vedic multiplier proves to be highly efficient in terms of speed. A complete study and layout analysis for 4 Bit Ripple Carry Adder are done and also their parameters were compared. In future we will concentrate on 8Bit Ripple Carry Adder using 4x4 UT Multiplier.

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