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Design and development of CPLD based image acquisition system

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***Abstract*—This paper deals with the design and development of CPLD based an image acquisition system. In this system, the area under surveillance is continuously monitored by taking the video of the place. This is accomplished by using the CMOS sensor, which captures the image frames. CMOS sensor and pixel data interface are connected to the CPLD through I2C bus. The CPLD device used in the present work is MAX V (5M2210Z) manufactured by Altera. Quartus II 13.0 suite is used for software development. CPLD will be programmed with the help of Verilog HDL.VGA Controller module in the CPLD will read the pixel data from the memo and it can display the image on LCD monitor.**

***Index Terms*—CMOS sensor, CPLD, VGA controller, LCD monitor**

I. INTRODUCTION

Advances in CPLD technology have dramatically increased the use of CPLDs for computer vision applications [1]. With the advent of today's highly integrated CPLD it is possible to have a software programmable processor and hardware computing resources on the same chip [2]. Apart from having enough logic blocks on which the hardware is implemented these chips also have an embedded processor with system software to implement the application software around it [3]. CPLD-based embedded systems are of increasing importance especially in the signal and image processing domain [4]. For instance, intelligent embedded systems for image processing, such as smart cameras, rely on CPLD-based architectures [5]. One of the most important advantages of the CPLD is the ability to exploit the inherently parallel nature of many vision algorithms [6]. The role of CPLD in embedded systems is gaining importance due to its increasing capabilities and availability of powerful Electronic Design Automation (EDA) tools [7]. The amount of resources in today's CPLDs is quite high and can practically handle many processing operations. Data coming from the sensor or any acquisition device is directly processed by the CPLD; no other external resources are necessary [8].

CPLD technology is become an alternative for the implementation of software algorithms. The unique structure of the CPLD has allowed the technology to be used in many applications from video surveillance to medical imaging applications. CPLD is a large-scale integrated circuit that can be re-programmed [9]. Implementations of real-time image processing algorithms can be done on general purpose microprocessors. In certain instances, image processing algorithms are also implemented using digital signal processors and application specific integrated circuits [10]. The application of CPLD in image processing has a large impact in the application of CPLDs in image or video processing. This is due to the potential of the CPLD to have parallel and high computational density as compared to a general-purpose microprocessor. This is coupled together with the ability of CPLD of being re-programmable that adds flexibility in the development of image processing algorithms on CPLD [11]. A CMOS camera captures images or streaming a video and converts them into digital, processes and interprets the data that it acquires in real-time [12].

II. HARDWARE SPECIFICATIONS

A. CMOS image sensor

The Micron Imaging MT9M011 is an SXGA-format, 1/3-inch CMOS active-pixel digital image sensor with an active imaging pixel array of 1,280H x 1,024V. It incorporates advanced camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface and has low power consumption [13]. The megapixel CMOS image sensor features Digital-Clarity Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS [14]. The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs an SXGA image at 13.9 frames per second

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(fps). It's operating temperature range from -30^{0}C to +70^{0}C. It requires small supply voltage: 2.8V ±0.3V. Its power consumption will be very low and is ideal for battery operated devices. This CMOS sensor will produce direct digital output because its associated circuit is incorporated with ADC. The photograph of the CMOS sensor with internal ADC circuit is shown in Fig1. Construction of CMOS camera is shown in Fig.2. The black diagram of CMOS camera with ADC circuit is shown in Fig3.

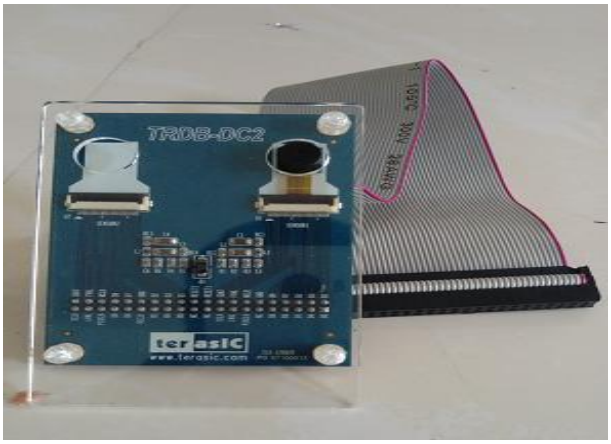

Fig1. Photograph of the CMOS sensor with ADC

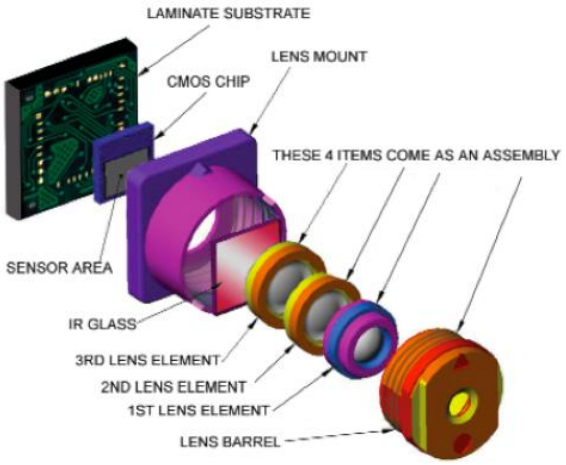

Fig2. Construction of CMOS camera

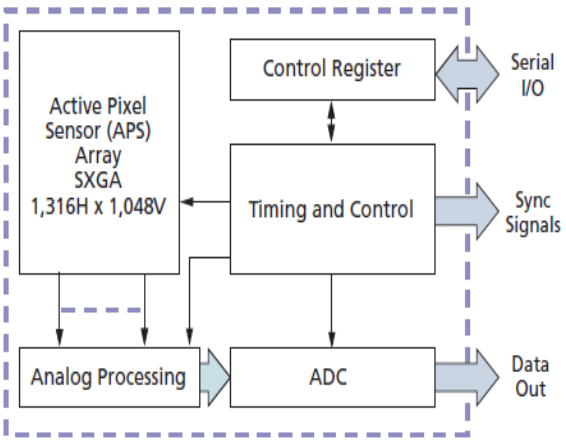

Fig3. Black diagram of CMOS camera with ADC circuit

B. CPLD (COMPLEX PROGRAMMABLE LOGIC DEVICE)

Application designers will configure the CPLDs to enforce digital hardware such as mobile phones. CPLDs are another way to extend density of the simple PLDs. The concept is to have a few functional blocks or PLD blocks or macro cells on a single device with general purpose interconnect in between. The macrocell is the building block of CPLD. This macrocell consists of specific logic operations and logic implementing disjunctive normal form expressions. CPLD's are ideal for critical, high-performance control applications, because of their inevitable timing characteristics [15]. When compared to FPGAs and other programmable logic devices CPLDs have a shorter and more predictable delay. CPLDs are inexpensive and need relatively small amounts of power; they are frequently used in cost-effective, battery-operated portable applications. The CPLD device used in the present work is MAX V (5M2210Z) manufactured by Altera. When compared to other competitive CPLDs, MAX V offers less in cost, consumes less power and provides more I/O pins. MAX V CPLDs have non-volatile architecture and one of the industry's largest densities. Many functions such as flash, RAM, oscillators, and phase-locked loops are integrated within the MAX V. With help of green packaging technology, MAX V has the packages as small as 20 mm. MAX V CPLDs are supported by Quartus II software v.13.0, which allows productivity enhancements resulting in faster simulation, faster board bring-up, and faster timing closure. The design can be implemented on different nano-chips for better efficiency depending upon the design requirement [16].

C. VGA (VIDEO GRAPHICS ARRAY)

VGA is referred to as an "array" instead of an "adapter" because it was implemented from the start as a single chip (an ASIC), replacing the Motorola 6845 and dozens of discreet logic chips that covered the full-length ISA boards of the MDA, CGA, and EGA. Its single-chip implementation also allowed the VGA to be placed directly on a PC's motherboard with a minimum of difficulty (it only required video memory, timing crystals and an external RAMDAC), and the first IBM PS/2 models are equipped with VGA on the motherboard.

D. I2C PROTOCOL

I²C bus is an abbreviation for Inter Integrated Circuit bus. It is also known as IIC and I2C. I²C is a serial and synchronous bus protocol. In standard applications hardware and timing are often the same. The way data is treated on the I²C bus is to be defined by the manufacturer of the I²C master and slave chips. In a simple I²C system there can only be one master, but multiple slaves. The difference between master and slave is that the master generates the clock pulse. The master also defines when communication should occur. For bus timing, it is important that the slowest slave should still

be able to follow the master's clock. In other words, the bus is as fast as the slowest slave.

E. IMAGE ACQUISITION SYSTEM

In this system, the CMOS sensor is continuously monitoring its surrounding area by taking the video of the place, which captures the image frames. The CMOS image sensor circuitry has internal Analog to Digital Converters to capture digital pixel values. It is having various configurable settings to adjust image resolution, brightness and contrast. The CMOS sensor is configurable to the desired resolution and exposure settings. These settings are done by programming the mode register of the sensor. In order to program the mode register, I2C protocol is used. Using this, the programming data is transferred to the sensor. The parallel data available is converted into serial data and is transferred to the sensor. The programmed sensor captures data continuously. CMOS sensor's I2C interface and Pixel Data interface are connected to the CPLD through GPIO interface of the MAX V board. CPLD will have I2C slave controller module that will write the CMOS sensor configurable register values. Since the sensor captures video continuously, it is necessary to control the flow of data to the memory where it is stored. Hence the Image Data Flow Controller is used. It specifies the start and stop to store data. It regulates the flow of data to the memory. The data is stored only when start signal is activated. It is continuously done till stop signal is encountered. The data is stored in the form of black and white image. For this, the black and white converter module is used. The captured image frames are stored in the memory and the video can be monitored on a visual display unit such as an LCD monitor. Fig.4 shows real-time video capturing and displaying on the monitor through CMOS camera connected with CPLD board.

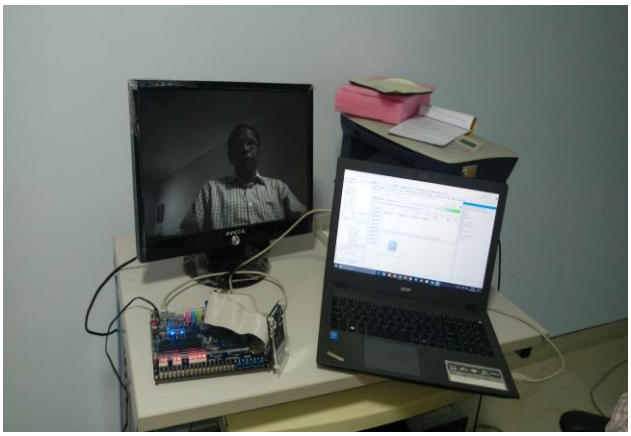

Fig.4 Photograph of the Image Acquisition system

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