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A VERILOG IMPLEMENTATION OF RING OSCILLATOR USING LCA & HRA APPROACHES FOR BIST SCHEMES

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Abstract— **The generation of significant power droop during at speed test performed by logic BIST. we have discusses in two approaches to reduce the PD generated at capture during at-speed test of combinational and sequential circuits with scan-based Logic BIST using the Launch-On-Shift scheme. both approaches increase the correlation between adjacent bits of the scan chains with respect to conventional scan-based LBIST. First approach hereinafter referred to as Low-Cost Approach (LCA), enables a reduction in the worst case magnitude of PD during conventional logic BIST.LCA features a comparable AF in the scan chains at capture, while requiring lower test time and area overhead. The second approach, hereinafter referred to as High-Reduction Approach (HRA), enables scalable PD reductions at capture, with limited additional costs in terms of area overhead and number of required test vectors for a given target FC, over our LCA approach. HRA enables a significantly lower AF in the scan chains during the application of test vectors. The proposed method of ring oscillator and carry save adder is used. The testing method is implemented in combinational logic of carry save adder. So we have to reduce power droop and calculate the power, area and delay.**

Index term: Logic BIST, Power Droop, Test, Microprocessor, carry save adder

I INTRODUCTION

The Continuous scaling of microelectronic technology enables to keep on increasing ICs' integration density and performance. This comes together with new challenges for system test and reliability. high performance sequential ICs using scan, the IC activity factor (AF) induced by the applied test vectors is significantly higher than that experienced during its in field operation .Consequently, power droop (PD) may take place during both shift and capture phases, which will slow down the circuit under test (CUT) signal transitions. the power consumption of BIST is used to minimize the area and no loss of fault coverage[1,2].low power test pattern generator based on a modified LFSR. A novel 2-dimensional programmable logic BIST can generate the desired speed.[3,4,6]. As a result, a false test fail may be generated, with consequent increase in yield loss[2,3].low frequency and high frequency power droop testing method is used for ATPG Algorithm such as PODEM(path oriented decision making)[5].

A test pattern generator with a pre-selected toggling level (PRESTO) [9] is presented. It enables to scale the AF reduction in the scan chains by preselecting the number of shift cycles during which they are loaded with constant logic values. two basic capture-clocking schemes exist the launch-on-shift (LOS) scheme, and the launch-on-capture (LOC) scheme [14,16]. In the LOS scheme, the test vectors are applied to the CUT at the last shift clock (CK) of the shift phase, and the CUT response is sampled on the scan chains at the following capture cycle. In the LOC scheme, instead, the test vectors are first loaded into the scan-chains during the shift phase, then, at the following capture cycle, the test vectors are applied to the CUT, and the CUT response is captured on the scan chains at a subsequent, second, capture cycle. In this paper we consider the case of sequential CUTs with scan-based LBIST adopting a LOS scheme. BIST scheme is presented and its effectiveness is studied over a differential ring oscillator.

The CUT/DFT structure generates a single Fail/Pass signal when in Test Mode which can be further processed by a standard digital process controller. the carry save adder is used to test the combinational logic generate and propagate method. Carry Save Adder (CSA) is the high speed multi operand adder used in many applications. To avoid this problem when at-speed testing is per-formed by an ATE, some ATPG approaches have been Proposed[11,12]. They use don't care bits (X) to reduce the AF at capture induced by the applied test vectors. However, due to the increasing costs of ATE and the rapidly evolving microelectronic technology, at speed testing of logic blocks is now a days frequently performed using Logic Built-In Self-Test (LBIST). Both

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combinational and scan-based LBIST schemes suffer from the PD-induced problem at capture described above. In case of scan-based LBIST, two basic capture-clocking schemes exist the launch-on-shift (LOS) scheme, and the launch-on-capture (LOC) scheme [14,16]. In the LOS scheme, the test vectors are applied to the CUT at the last shift clock (CK) of the shift phase, and the CUT response is sampled on the scan chains at the following capture cycle.

Based on these considerations, in this paper w e pro-pose two approaches to reduce the PD at capture of sequential circuits with scan-based Logic BIST with Launch-On-Shift scheme. The basic idea behind our approaches, which has been introduced in [20], is to increase the correlation between adjacent bits of the scan chains with respect to conventional scan-based LBIST. This w ay, at capture, the AF of the scan chains is reduced with respect to conventional scan-based LBIST. As a consequence, the AF of the CUT at capture, thus the PD at capture, is also reduced compared to conventional scan-based LBIST. This solution [17] does not impact the fault coverage and can be employed during scan-based LBIST, for both LOC and LOS schemes. However, it increases test time, as well as the total power consumed during test, with its associated negative thermal effects. we recently proposed an approach to reduce PD at capture in scan-based LBIST adopting the LOC scheme.

It enables to reduce PD at capture up to the 50%compared to conventional scan-based LBIST by replacing one test vector of the test sequence with a substitute test vector that increases the correlation between the test vectors applied at following capture cycles. However, this approach does not increase the correlation between adjacent bits of the scan chains, so that it is not effective in reducing PD at capture in scan-based LBIST adopting the LOS scheme. the remainder of the paper is organized as follows. in section 2, we describe the considered, conventional scan-based LBIST. In Section 3, w e introduce our proposed approaches for PD reduction at capture. In Section 4, w e show a comparison of area, delay and power. In Section 5, shows experimental results. In section 6 concludes the paper.

II EXISTING METHOD

In Existing, An Approach To Reduce PD At Capture In Scan Based LBIST Adopting The LOC Scheme. It Enables To Reduce PD At Capture Up To The Compared To Conventional Scan-Based LBIST By Replacing One Test Vector Of The Test Sequence With A Substitute Test Vector That Increases The Correlation Between The Tests Vectors Applied At Following Capture Cycles. However, This Approach Does Not Increase The Correlation Between Adjacent Bits Of The Scan Chains, So That It Is Not Effective In Reducing PD At Capture In Scan Based LBIST Adopting The LOS Scheme.

In this section, we introduction two approaches. Our first approach, hereinafter referred to as Low-Cost Approach(LCA), enables a reduction of the PD at capture up to the half with respect to conventional scan-based LBIST. It requires a small cost in terms of area overhead, and does not in-crease the number of test vectors over those required by conventional scan-based LBIST to achieve the same FC. In particular, during the shift phase, the phase shifter provides a new bit to each one of the s scan chains (in parallel)at each shift CK. As represented in Fig. 1, when employing a LOS scheme, the scan enable(SE) signal must switch to 0 between the last shift CK and the following capture cycle. We refer to the case where the shift CK presents a lower frequency than the capture CK, to reduce power consumption. In the LOS scheme [16], the delay effect produced by the CUT AF that can be erroneously recognized as a delay fault occurs at capture, that is between the last shift CK and the following capture cycle.

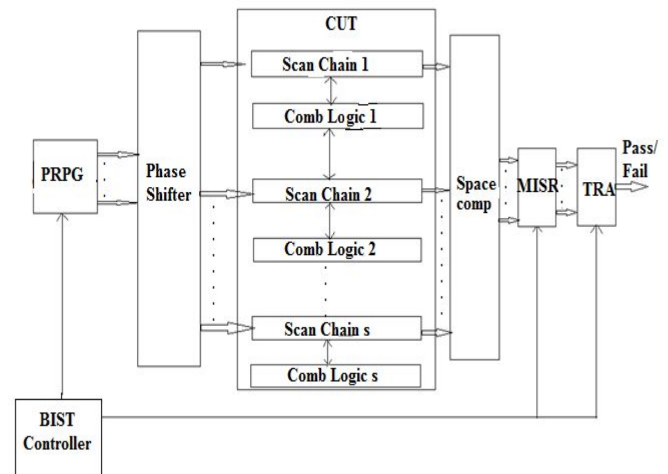

Fig 1. Schematic Representation of The Scan Based LBIST Architecture

Our second solution, hereinafter referred to as High-Reduction Approach(HRA), relies on further increasing the correlation between adjacent bits of the scan chains compared to LCA. It enables scalable reductions of the PD at capture up, thus allowing maximal flexibility to the test development team concerning the PD to induce during test, in order to avoid false test fails. This is achieved at limited additional cost over LCA. In the LOS scheme False test fail may be generated, with consequent increase in yield loss. it requires a significant increase in number of test vectors consequently test time, to achieve the same Fault Coverage (FC)as with conventional scan-based LBIST.

The MISR generates a signature after the application of all test vectors, which is then compared to the expected one by the Test Response Analyzer (TRA). Finally, the BIST Controller controls all operations during scan-based LBIST. LBIST employing a LOS scheme [16]. Two phases can be identified. A shift phase, consisting of n shift CKs(where n is the number of scan flip-flops in the longest scan chain), during which the scan chains are filled in with test vectors, which are applied to the CUT at the last (n-th) shift CK. a capture phase, consisting of a single capture clock, in which the CUT response to the test vectors applied at the last shift
CK is sampled. Then, other n scan shift CKs are required to shift-out the CUT response and to shift-in the new test vector.

In particular, during the shift phase, the phase shifter provides a new bit to each one of the s scan chains (in parallel)at each shift CK. As represented in Fig. 1, when employing a LOS scheme, the scan enable(SE) signal must switch to 0 between the last shift CK and the following capture cycle. We refer to the case where the shift CK presents a lower frequency than the capture CK, to reduce power consumption. In the LOS scheme [16], the delay effect produced by the CUT AF that can be erroneously recognized as a delay fault (with the consequent generation of a false test

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fail)occurs at capture, that is between the last (n-th) shift CK and the following capture cycle.

III PROPOSED METHOD

The state flip-flops of the CUT are converted into scan flip-flops and arranged into many short scan chains. Additional scan flip-flops are included in order to drive and sample primary inputs (PI) and primary outputs (PO).The pseudo random pattern generator is replaced by ring oscillator. A ring oscillator is a circuit which consists of an odd number of inverter stages, where the output on each stage of the ring oscillator is given to the input of next stage and output of final stage is then fed to its input. Also, no external input is given to the device, only a reset pulse is provided at once and it drives the circuit.

Ring oscillators are fabricated using System on Chip designs as they occupy less chip area thereby improving both the cost and yield. a DFT solution for the testing of ring oscillators has been proposed . The CUT/DFT structure generates a single Fail/Pass signal when in Test Mode which can be further processed by a standard digital process controller. The Phase Shifter (PS), enabling to reduce the correlation among the test vectors applied to adjacent scan-chains, consists of an XOR network expanding the number of outputs of the LFSR in order to match the number of scan chains s. At the same clock cycle(CK), the PS pro-vides as outputs the current LFSR sequence together with many future/past sequences .

The CUT of scan chain and combinational logic of carry save adder is used to test the current, the fault will be detected. The carry save adder is a high speed multi operand adder used in many application.The Space Compactor compacts the outputs of the scan chains to match the number of inputs of the MISR. The MISR generates a signature after the application of all test vectors, which is then compared to the expected one by the Test Response Analyzer (TRA). Finally, the BIST Controller controls all operations during scan-based LBIST. LBIST employing a LOS scheme

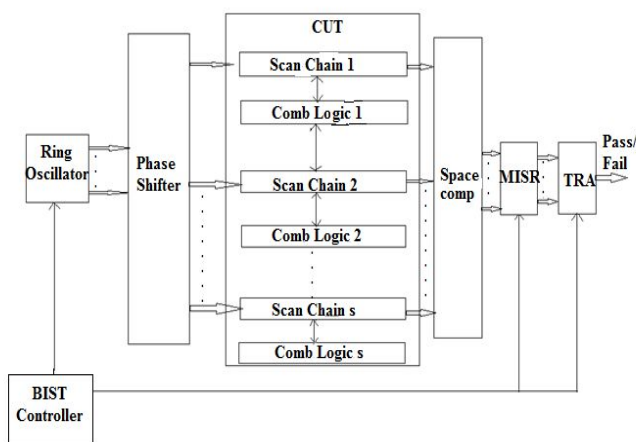

Fig 2. Proposed Method of Scan Based LBIST Architecture

A. LOW COST APPROACH

The proposed hardware implementation is represented, scan chain *m*, our approach requires 1 multiplexer (M 1), a 2-input AND, and a 2-input XOR. At each shift CK, M 1 allows to load in the scan chain *m*: 1) the bits given on the PS output O^m w hen *sel*=0; 2) bits with a random value *R*, w hen *sel*=1. When the control signal *int* is 0, the AN D gate allow s to make *sel*=0, thus loading into the scan chain *m* the bits given on the PS output O^m. Instead, when *int*=1, depending on the value of the *mod* signal generated by the XOR gate, M1 selects w hether to drive the logic value on O^m or the random value *R* in the scan chain *m*. The signal *int* must be equal to 0 in the first shift CK in order to load into the scan chain the first unmodified bit, as required by our approach. Then, in the remaining *n-1* shift CKs, the signal *int* is equal to 1 in order to enable to modify the bits to be loaded into the scan chain *m*, w hen required by our approach.

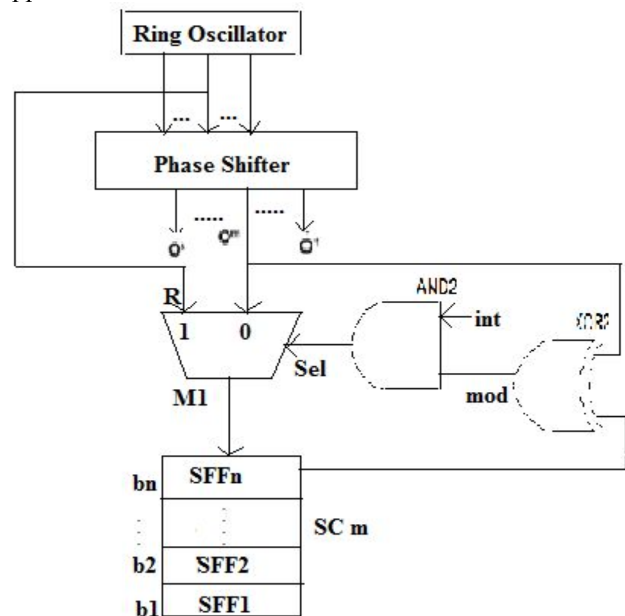

Fig 3. Low cost approach

B. HIGH REDUCTION APPROACH

scan chain *m*, our approach requires 2 multiplexers (M 1 and M 2), a 2-input AN D, and a 2-input XOR. As for the LCA implementation, M 1 allow s to select: 1) the bits given on the PS out-put O^m, w hen *sel*=0; 2) bits with a random value *R*, w hen *sel*=1. The AND gate enables to make *sel*=0, thus loading into the scan chain the bits given on the PS output O^m, w hen *int =0*. Instead, w hen *int=1,* depending on the value of the *mod* signal (that is generated at the XOR gate out-put), M 1 selects the logic value on O^m or the *R* bit. There-fore, bits at the M 1 output are modified as required to implement the methodology *M et2* described before.

Moreover, at each shift CK, M 2 allow s to load in the scan chain *m*: 1) the bits given at the M 1 output, w hen control signal *rep*=0; 2) the bit b_n at the output of the first scan flip-flop (SFF_n) of the scan chain, w hen *sel*=1. This w ay, w hen *sel=0*, M 2 selects to load in the scan chain bits modified by *M et2*. Instead, w hen *sel*=1, M 2 selects to load in the scan chain the same bit loaded at the previous shift CK, that is bits modified by *M et1*. As described before for the LCA , the bit *R* can be simply generated from any output of the Ring oscillator.

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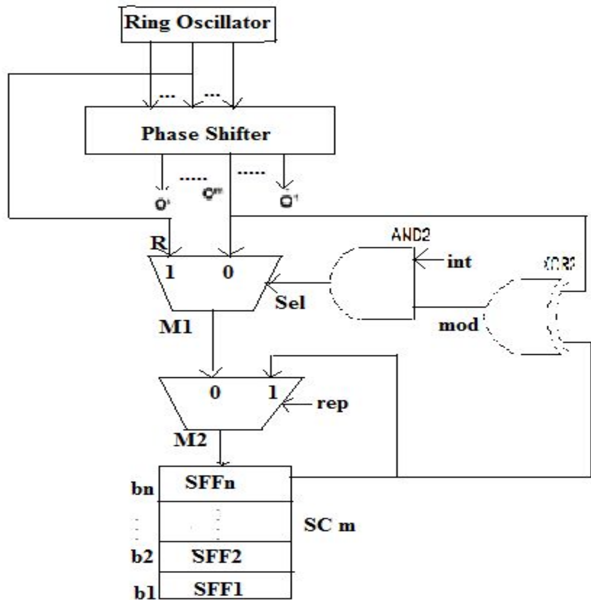

Fig 4. High Reduction Approach

IV COMPARISON

We have compared the effectiveness of our LCA and HRA with those of Conventional LBIST [13], and those of the three recent alternate solutions in [2, 6, 9] for the reduction of PD at capture in scan-based LBIST using the LOS scheme. Effectiveness has been evaluated in terms of allowed PD reduction at capture and number of test vectors required to achieve a target stuck-at FC, which can still be considered a good metric for test quality. The low cost approach and high reduction approaches are designed to test the combinational logic of the carry save adder circuit. The ring oscillator is also used to calculate the power, area and delay.

Method	Power	Area	Delay
Existing method of LCA	5417 mW	478	11.673ns
Proposed method of LCA	3719 mW	377	12.994ns

Table 1.Comparision of LCA

Method	Power	Area	Delay
Existing method of LCA	4702mW	619	11.673ns
Proposed method of LCA	2512mW	518	12.994ns

Table 2.Combarison of HRA

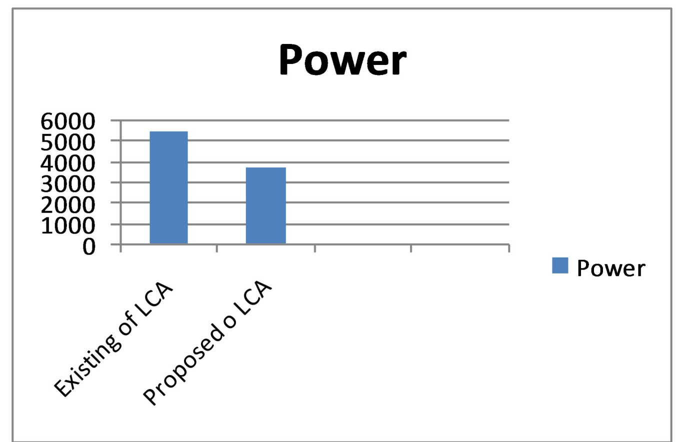

Fig 5. Graphical representation of LCA Power

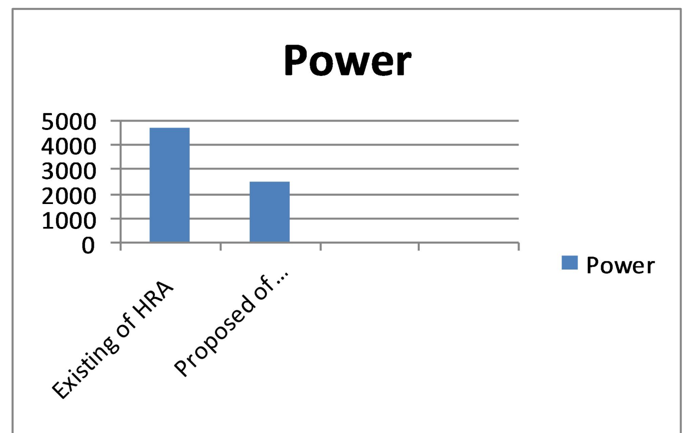

Fig 6. Graphical representation of HRA Power

V RESULT

The Low cost approach and High reduction approaches are implemented. It has been seen that the power Droop is reduced by the Low cost approach. The proposed method of ring oscillator and carry save adder is implemented.the testing method is implemented in combinational logic of carry save adder. the power consumption, area and delay is reduced.

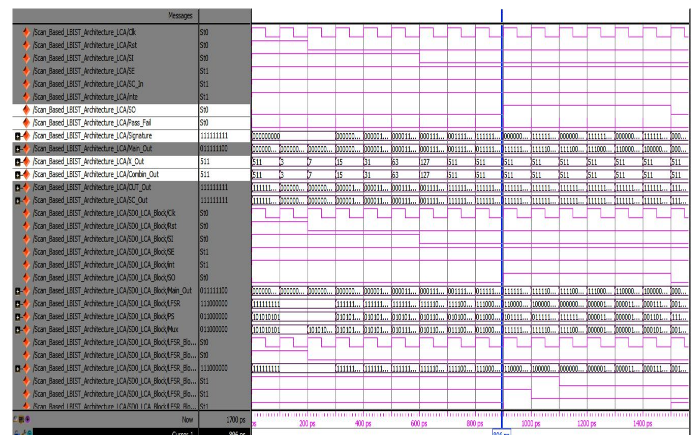

Fig 7. Scan based architecture of LCA

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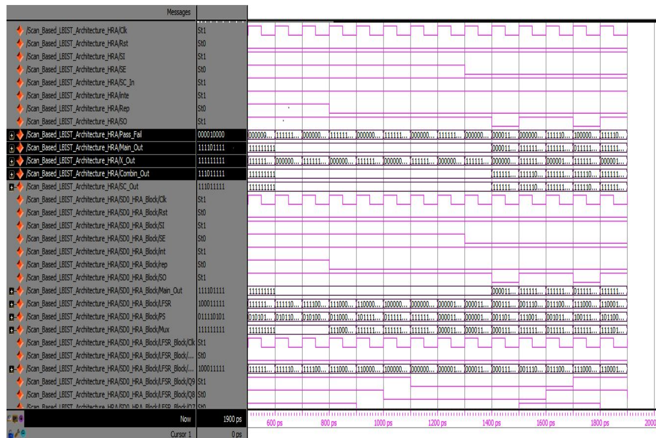

Fig 8. Scan based architecture of HRA

VI CONCLUSION

we have discusses in two approaches to reduce the PD generated at capture during at-speed test of combinational and sequential circuits with scan-based Logic BIST using the Launch-On-Shift scheme. both approaches increase the correlation between adjacent bits of the scan chains with respect to conventional scan-based LBIST. First approach hereinafter referred to as Low-Cost Approach (LCA), enables a reduction of PD during conventional logic BIST, while requiring lower test time and area overhead. The second approach, hereinafter referred to as High-Reduction Approach (HRA), enables scalable PD reductions at capture, with limited additional costs in terms of area overhead and number of required test vectors for a given target FC, over our LCA approach. HRA enables a significantly lower AF in the scan chains during the application of test vectors. The proposed method of ring oscillator and carry save adder is used. The testing method is implemented in combinational logic of carry save adder. So we have to reduce power droop and calculate the power, area and delay. it is implemented in FPGA.

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