ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 5, May 2017

Design and Implementation of Low Power Programmable PRPG with Test Compression Capabilities

V.Ramyaparameswari
P.G Scholar,M.E-VLSI Design
Srinivasan Engineering College
Perambalur,Tamilnadu

Mr.D.Karthikeyan
Assistant Professor/Department of ECE
Srinivasan Engineering College
Perambalur,Tamilnadu

***Abstract*- This paper describes a low-power (LP) programmable generator capable of producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the built-in self-test (BIST)based pseudorandom test pattern generators.. Furthermore, this paper proposes an LP test compression method that allows shaping the test power envelope in a fully predictable in accurate manner and flexible by adapting the PRESTO-based logic BIST (LBIST) infrastructure. We introduce a method combinational C17 and sequential S27 bench mark circuit to automatically select several controls of the generator offering easy and precise tuning The proposed hybrid scheme with combinational and sequential circuit techniques to test the circuits and to deliver high quality tests.**

***Index Terms* –Built-in-self-test (BIST), low power test, pseudorandom test pattern generators(PRPG),testdatavolume compression.**

I.INTRODUCTION

Although over the next years, the primary objective of manufacturing test will remain essentially the same to ensure reliable and high quality semiconductor products conditions and consequently also test solutions may undergo a significant evolution. Test compression introduced a decade ago, has quickly become the main stream DFT methodology.

However, it is unclear whether test compression will be capable of coping with the rapid rate of technological changes over the next decade. Interestingly, logic built-in self-test (LBIST), originally developed for board, system, and in-field test, is now gaining acceptance for production test as it provides very robust DFT and is used increasingly often with test compression. This hybrid approach seems to be the next logical evolutionary step in DFT. It has potential for improved test quality, it may augment the abilities to run at-speed power aware tests, and it can reduce the cost of manufacturing test while preserving all LBIST and scan compression advantages. If BIST logic is used to deliver compressed test data, then underlying encoding schemes typically take advantage of low fill rates, as originally proposedinLFSR. Thorough surveys of relevant test compression techniques can be found. As with conventional scan-based test, hybrid schemes, due to the high data activity associated with scan-based test operations, may consume much more power than a circuit under- test was designed to function under.

II.FULLY OPERATIONAL PRESTO

In this paper, we used a PRPG for LP BIST applications. It can assume a variety of configurations that allow a given scan chain to be driven either by a PRPG itself or by a constant value fixed for a given period of time.

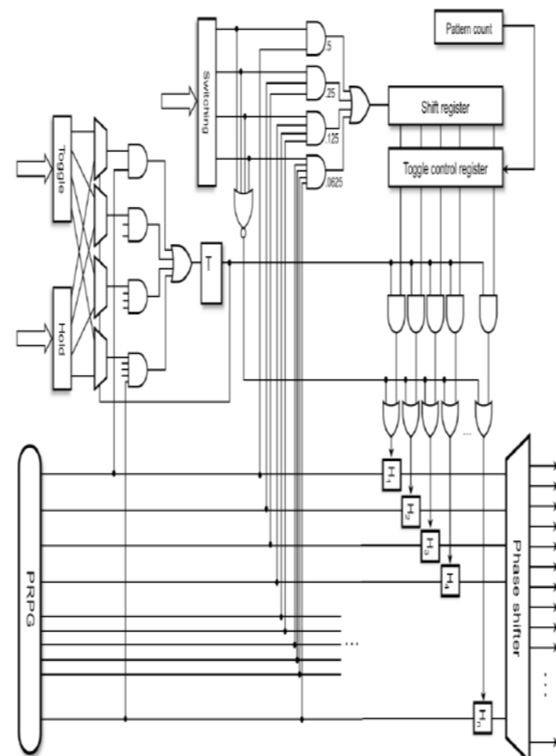

Fig 1:Fully Operational PRESTO

We will demonstrate that this flexible programming can be further used to produce tests superior to conventional pseudorandom vectors with respect to a resultant fault-coverage-to-test-pattern-count ratio. This paper culminates in showing that the PRESTO generator can also successfully

All Rights Reserved © 2017 IJARECE

act as a test data decompress or, thus allowing one to implement a hybrid test methodology that combines LBIST and ATPG-based embedded test compression.this approach splits up a shifting period of every test pattern into a sequence of alternating hold and toggle intervals. To move the generator back and forth between these two states, we use a T-type flip-flop that switches whenever there is a 1 on its data input. If it is set to 0, the generator enters the hold period with all latches temporarily disabled regardless of the control register content.

This is accomplished by placing AND gates on the control register outputs to allow freezing of all phase shifter inputs. This property can be crucial in SoC designs where only a single scan chain crosses a given core, and its abnormal toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods. If the T flip-flop is set to 1 (the toggle period), then the latches enabled through the control register can pass test data moving from the PRPG to the scan chains.

Two additional parameters kept in 4-bit Hold and Toggle registers determine how long the entire generator remains either in the hold mode or in the toggle mode, respectively. To terminate either mode, a 1 must occur on the T flip-flop input. This weighted pseudorandom signal is produced in a manner similar to that of weighted logic used to feed the shift register. The T flip-flop controls also four 2-input multiplexers routing data from the Toggle and Hold registers. It allows selecting a source of control data that will be used in the next cycle to possibly change the operational mode of the generator. For example, when in the toggle mode, the input multiplexers observe the Toggle register. Once the weighted logic outputs 1, the flip-flop toggles, and as a result all hold latches freeze in the last recorded state. They will remain in this state until another 1 occurs on the weighted logic output. The random occurrence of this event is now related to the content of the Hold register, which determines when to terminate the hold mode. When using the PRESTO generator with an existing DFT flow, all LP registers are either loaded once per test or every test pattern. The registers loaded only once act as test data registers.

III.LP DECOMPRESSOR

This is the first LP test compression scheme that is integrated in every way with the BIST environment and lets designers shape the power envelope in a fully predictable, accurate, and flexible fashion. As a result, it creates an environment that can be used to arrive at an efficient hybrid solution combining advantages of scan compression and logic BIST. In addition, both techniques can complement each other to address.In order to facilitate test data decompression while preserving its original functionality core principle of the decompressor is to disable both weighted logic blocks and to deploy deterministic control data instead. In particular, the content of the toggle control register can now be selected in a deterministic manner due to a multiplexer placed in front of the shift register. Furthermore, the Toggle and Hold registers are employed to alternately preset a 4-bit binary down counter, and thus to determine durations of the hold and toggle phases. When this circuit reaches the value of zero, it causes a dedicated signal to go high in order to toggle the T flip-flop. The same signal allows the counter to have the input data kept in the Toggle or Hold register entered as the next state. Both the down counter and the T flip-flop need to be initialized every test pattern.

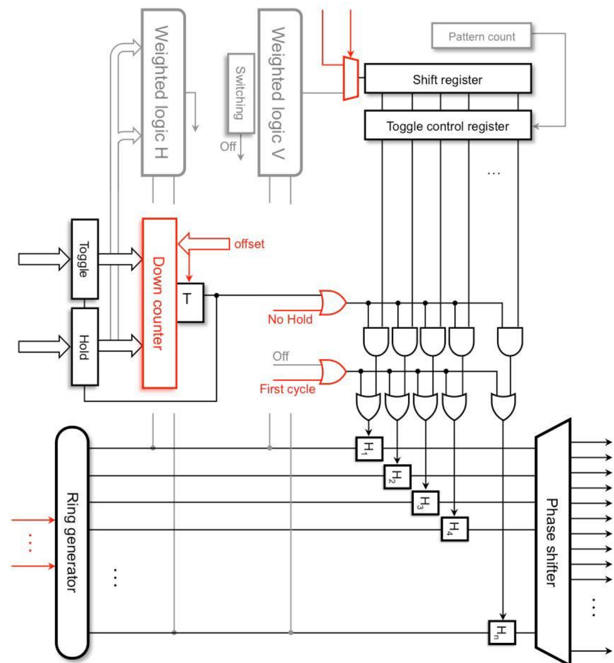

Fig 2: LP Decompressor

The initial value of the T flip-flop decides whether the decompressor will begin to operate either in the toggle or in the hold mode, while the initial value of the counter, further referred to as an offset, and determines that mode's duration. As can be seen, functionality of the T flip-flops remains the same as that of the LP PRPG but two cases. First of all, the encoding procedure may completely disable the hold phase (when all hold latches are blocked) by loading the Hold register with an appropriate code, for example, 0000. If detected it overrides the output of the T flip-flop by using an additional OR gate. As a result, the entire test pattern is going to be encoded within the toggle mode exclusively. In addition, all hold latches have to be properly initialized. Hence, a control signal First cycle produced at the end of the ring generator initialization phase reloads all latches with the current content of this part of the decompressor.

IV.BENCHMARK CIRCUIT

The ITC'02 SOC Test Benchmarks is a set of benchmark circuits with a special focus on modular plug-and-play testing of core-based system chips.The purpose of these benchmark circuits is to stimulate research in new methods and tools for modular testing of core-based SOCsand to enable the objective comparison of such methods and tools with respect to effectiveness and efficiency.

All Rights Reserved © 2017 IJARECE

A.MOTIVATION AND BACKGROUND:

With the ITC'02 SOC Test Benchmarks, we intend to combine the homogenity of the ISCAS'85 and ISCAS'89 benchmark circuits with the industrially-relevant sizes and characteristics of the ITC'99 benchmark circuits. On the one hand, we want to limit the amount of intellectual property that is released through the benchmarks, such that it will be easy for companies and other organizations to contribute one or more SOC designs to the benchmark set. On the other hand, we want to make sure that the information released contains sufficient data to solve relevant research problems in the SOC test automation domain, such as wrapper design, / TAM design, and test scheduling. We believe we have found a format, that fulfills the requirements above. This format describes the core design hierarchy. For each core, the number of terminals, core-internal scan chains, length of these chains, number of tests and test patterns per test are provided. Optionally, the power dissipation during a test, as well as the layout coordinates of the cores might be provided. Note that the contents of the cores and SOC are not provided; also the test patterns themselves are not provided. Furthermore, the cores are numbered, and hence their original names are also not provided.

B.COMBINATIONAL AND SEQUENTIAL CIRCUITS:

We can generally divide digital circuits into 2 subcategories: combinational and sequential. Combinational circuit means there's no memory element in the circuit. The logic is purely combinational. Figure 3.shows a common combinational circuit with several primary inputs (PI) and primary outputs (PO). If input vectors (logic 0s and 1s) are applied at PIs.

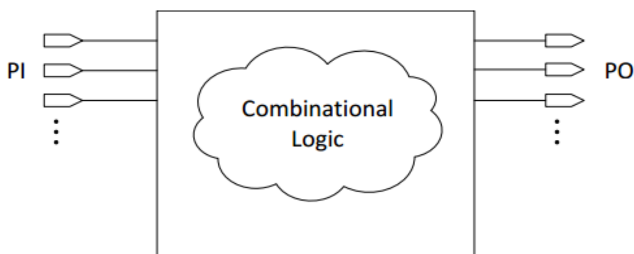

Fig 3: Combinational circuit

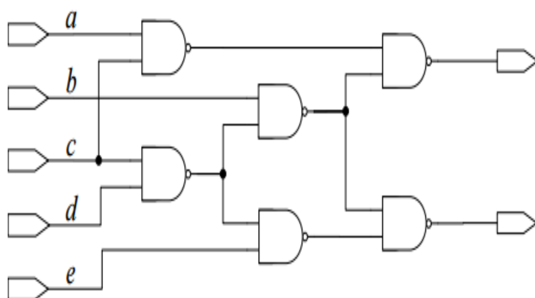

Fig 4: C17 Benchmark circuit

The outputresponses can be observed immediately at POs (after any gate delays). shows a simple example of a combinational circuit. If we apply a test vector "01010" at the primary inputs we should get "11" if the circuit functions correctly.

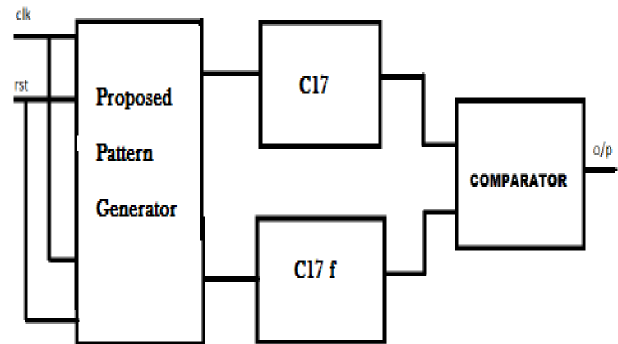

Fig 5: C17 Block diagram

Actually nearly all digital designs are sequential, i.e. there are flip-flops and/or other state holding elements inside the circuit. Introducing memory elements such as D flip- flops and latches makes it possible to reuse logic and hold state, which can extend the functionality of the circuit tremendously.

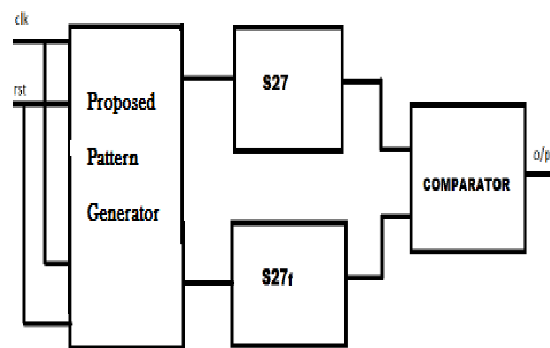

Fig 6: S27 Block diagram

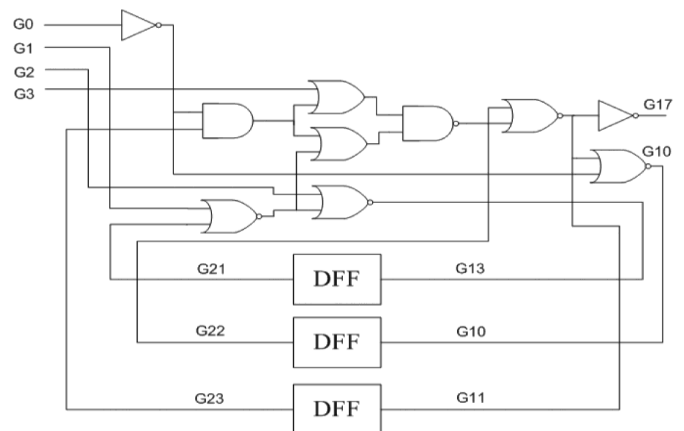

Fig 7: S27 Benchmark circuit

All Rights Reserved © 2017 IJARECE

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 5, May 2017

Circuit/Device under test (CUT/DUT) is exercised by applying test signals to its inputs.Output responses are observed and compared. If there's no mismatch between observed response and stored correctresponse, the CUT is considered good, otherwise it will be labeled as bad.

The input data to the CUT is referred to as the test pattern or test vector. Usually tests applied during testing are for fault detection.

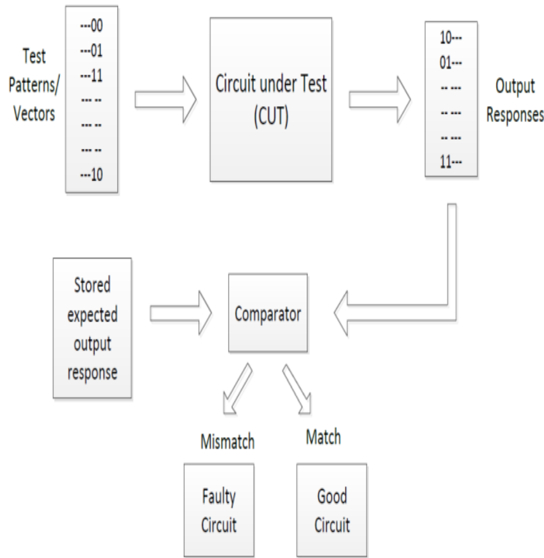

Fig 8:Circuit Under Test

The purpose of a detection test is to identify the CUT as faulty of fault-free. But in diagnosis, additional test patterns maybe applied, aiming to and the cause/location of the failure. Currently the available commercial silicon fabrication technology reduces the feature size down to 22nm .

Process variation has greater and greater impact on product quality. A manufactured circuit may develop various kinds of defects during and after the fabrication process.

Method	Area			Delay			Power
	LUT	Slices	Flip Flops	Delay (ns)	Logic Delay (ns)	Route Delay (ns)	(Mw)
Fully Operational Version PRESTO Generator	39	50	42	6.216	5.535	0.681	43
PRESTO Generator	32	52	51	7.165	6.364	0.801	43
Proposed LPD Compressor	32	52	51	7.165	6.364	0.801	41

Table 1:Comparison Table

V. OUTPUT

The combinational C17 and sequential S27 circuit of normal and fault circuit output.

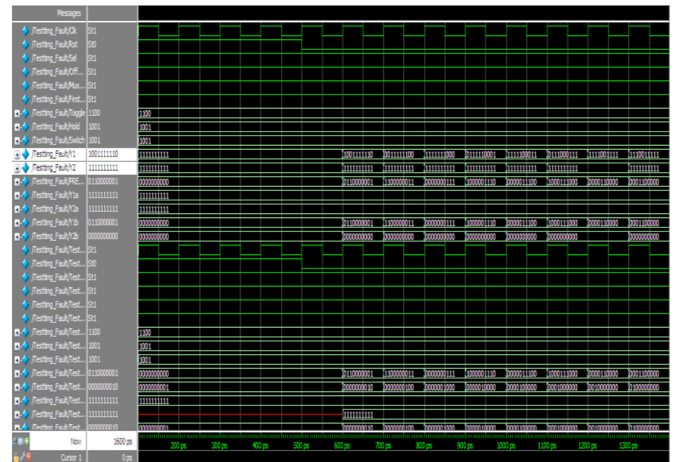

Fig 9: Combinational Testing of Normal Circuit

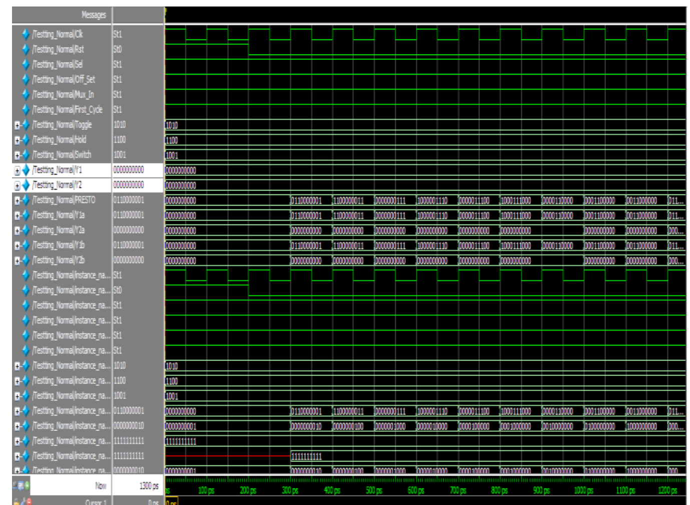

Fig 10:Combinational Testing of Fault circuit

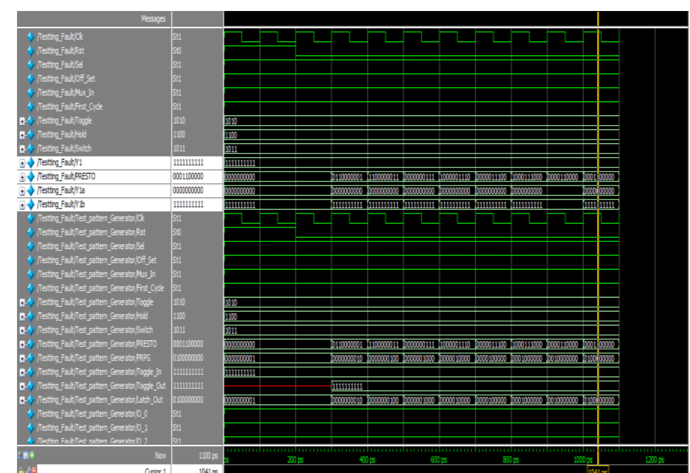

Fig 11: Sequential Testing of Normal Circuit

All Rights Reserved © 2017 IJARECE

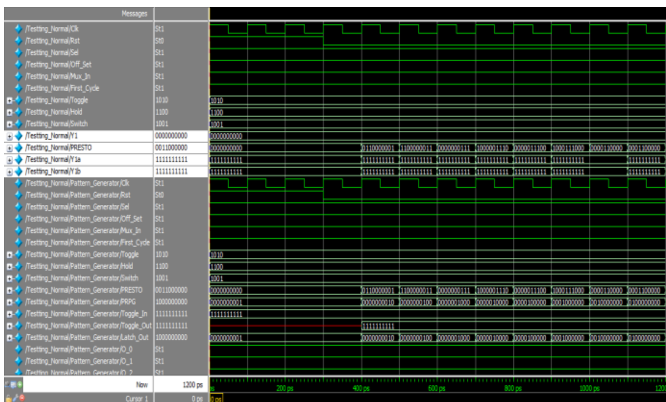

Fig 12: Sequential Testing of Fault circuit

VI.CONCLUSION

LPdecompressor method which allows combinational and sequential to test the fault and normal circuit of the circuit. This proposed work has the advantages of low power and less test application time.The method allow to automatically select several controls of the generator offering easy and precise tuning.

REFERENCES

[1] A. S. Abu-Issa and S. F. Quigley, "Bit-swapping LFSR for low-power BIST," Electron.Lett., vol. 44, no. 6, pp. 401–402, Mar. 2008.

[2] C. Barnhart et al., "Extending OPMISR beyond 10x scan test efficiency," IEEE Design Test, vol. 19, no. 5, pp. 65–73, Sep./Oct. 2002.

[3] S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, "Low-power scan design using first-level supply gating," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 3, pp. 384–395,Mar. 2005.

[4] M. Chatterjee and D. K. Pradham, "A novel pattern generator for nearperfectfault coverage," in Proc. 13th IEEE Very Large Scale Integr. (VTSI) Test Symp., Apr./May 1995, pp. 417–425.

[5] F. Corno, M. Rebaudengo, M. S. Reorda, G. Squillero, and M. Violante, "Low power BIST via non-linear hybrid cellular automata," in Proc. 18th IEEE Very Large Scale Integr. (VTSI) Test Symp., May 2000, pp. 29–34.

[6] D. Das and N. A. Touba, "Reducing test data volume using external/ LBIST hybrid test patterns," in Proc. Int. Test Conf. (ITC), 2000, pp. 115–122.

[7] R. Dorsch and H. Wunderlich, "Tailoring ATPG for embedded testing," inProc. Int. Test Conf. (ITC), 2001, pp. 530–537.

[8] M. Filipek et al., "Low power decompressor and PRPG with constant value broadcast," in Proc. 20th Asian Test Symp. (ATS), Nov. 2011, pp. 84–89.

[9] S. Gerstendorfer and H. Wunderlich, "Minimized power consumption for scan-based BIST," in Proc. Int. Test Conf. (ITC), 1999, pp. 77–84.

[10] V. Gherman, H. Wunderlich, H. Vranken, F. Hapke, M. Wittke, and M. Garbers, "Efficient pattern mapping for deterministic logic BIST," in Proc. Int. Test Conf. (ITC), Oct. 2004, pp. 48–56.

[11] P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A test vector inhibiting technique for low energy BIST design," in Proc. 17th IEEE VLSI Test Symp. (VTS), Apr. 1999, pp. 407–412.

[12] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H.-J.Wunderlich, "A modified clock scheme for a low power BIST test pattern generator," in Proc. 19th IEEE VLSI Test Symp. (VTS), May 2001, pp. 306–311.

[13] P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel, and H.-J.Wunderlich, "High defect coverage with low-power test sequences in a BIST environment," IEEE Design Test, vol. 19, no. 5, pp. 44–52, Sep. 2002.

[14] P. Girard, N. Nicolici, and X. Wen, Ed., Power-Aware Testing and Test Strategies for Low Power Devices. New York, NY, USA: Springer-Verlag, 2010.

[15] A.-W. Hakmi, S. Holst, H. Wunderlich, J. Schloffel, F. Hapke, and A. Glowatz, "Restrict encoding for mixed-mode BIST," in Proc. 27th IEEE VLSI Test Symp. (VTS), May 2009, pp. 179–184.

All Rights Reserved © 2017 IJARECE