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A study on implementing novel adder in HEVC DCT to achieve Area and Power Efficiency

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Abstract **-** No technologies are hundred percentage errors free. In modern VLSI technology, ineluctably error will occur. Implementation of integer discrete cosine transform (DCT) of all transform unit (TU) sizes, which can be used for high efficiency video coding (HEVC) also come under this. In this paper, a novel Error Tolerant Adder (ETA) is proposed which can provide great accuracy at its best; meanwhile provide enormous improvement in the area and the power consumption. It can provide area improvement of about 75.21% at the expense of an average error reading 12.46%. ETA provides more than 66.29% improvement in power consumption. The proposed technique is designed using XILINX ISE TOOL and coded by Verilog HDL language

Keywords **-** *Discrete cosine transform (DCT), H-265, High Efficiency Video Coding (HEVC), Error-Tolerant-Adder (ETA).*

I. INTRODUCTION

The main idiosyncrasy of Discrete Cosine Transform is its energy compaction property, which make it efficient for compression of video, especially in lossy-data compression. DCT is less complex as compared to DFT and FFT, can be performed in easier and more efficient way. DCT is considered as basis of the image compression standard issued by the Joint Photographic Experts Group (JPEG) [1].

All these made DCT suitable for transform in High Efficiency Video Coding (H.265), evolved from the existing video recommendations ITU-T H.264. Recommendation ITU-T H.265 is developed to meet the need for higher compression of videos in various applications such as internet streaming, communication, video conferencing, digital storage media and television broadcasting [2].

One of its relevant features is that it can support all TU sizes of DCT, i.e, HEVC standard uses 4x4, 8x8, 16x6 and 32x32 TU sizes for DCT. Larger TU sizes achieve better energy Thus, flexible efficient hardware architecture is used enough to compute all TU sizes, resource efficient and reusable with the same throughput. Here multiplication is replaced by adders, thus exist a plenty of adders. Possibilities of errors are not negligible [3].

The error-tolerant-adders are proposed to introduce at the place of each and every adders, to provide accuracy at its best at the same time shows an incomparable improvement in area and power consumption [4].

In section 2 a brief description about error-tolerant-adder is given. A detailed description about our proposed algorithm for implementation of integer discrete cosine transform for high efficiency video coding using error-tolerant-adder is given in section 3. The proposed architecture is implemented and obtained result is examined in section 4. Section 5 concludes on the paper proposed.

II. ERROR-TOLERANT-ADDER

The larger the input data set we have to enter is, the larger the adder should we choose. And if the output we should get at the same instant, the adder should be fast enough. The traditional fast adders like ripple-carry-adder (RCA), carry-skip adder (CSK), carry-select adder (CSL), carry-look-ahead adder (CLA), has its own disadvantages, as there are always trade-offs between speed and power.

The ETA can solve this entire problem, by sacrificing some accuracy leads to attain great improvement in both the power consumption and speed performance. The delay in adder is mainly due to carry propagation chain along critical path from LSB to MSB, resulting glitches lead to significant power consumption.

Thus eliminating carry propagation provide

great improvement in speed performance and power consumption; the main agenda of ETA.

Input data to be given is split into two parts: an accurate part and an inaccurate part provided no necessary to maintain the length of both part equal. From the middle addition starts, proceed toward the two opposite direction simultaneously. The example is given in Fig. 1

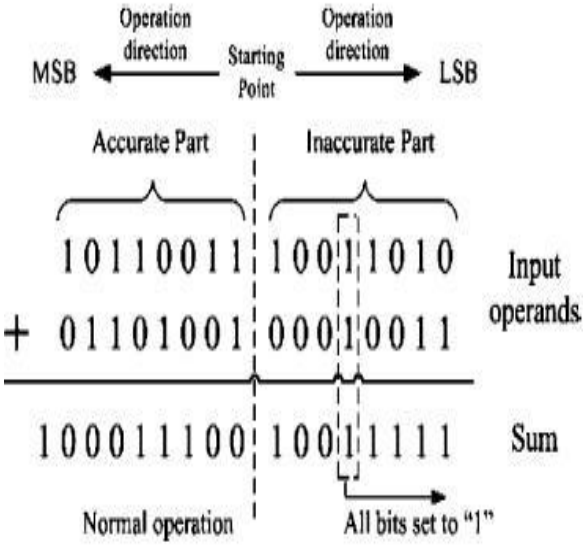

Fig1. ETA Architecture.

In the example of Fig. 1, the two 16-bit input operands, are divided equally into 8 bits each for the accurate and inaccurate parts. The addition of the higher order bits (accurate part) of the input operands is performed from right to left (LSB to MSB) and normal addition method is applied.

This is to preserve its correctness since the higher order bits play a more important role than the lower order bits. The lower order bits of the input operands (inaccurate part) require a special addition mechanism [6]. No carry signal will be generated or taken in at any bit position to eliminate the carry propagation path.

To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted, and can be described as follow:

1) Check every bit position from left to right (MSB to LSB);

2) If both input bits are "0" or different, normal one-bit addition is performed and the operation proceeds to next bit position**;**

3) If both input bits are "1," the checking process stopped and from this bit onward, all sum bits to the right are set to "1".

By eliminating the carry propagation path in the inaccurate part and performing the addition in two separate parts simultaneously, the overall delay time is greatly reduced, so is the power consumption.

II. ALGORITHM FOR IMPLEMENTATION OF DCT USING ETA

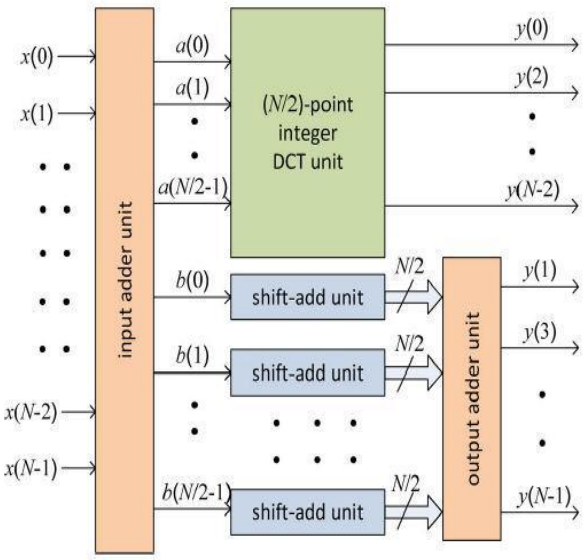

Fig.2 reusable DCT architecture for N = 4,8,16 and 32

The proposed reusable architecture for the implementation of DCT of any of the prescribed lengths is shown in Fig. 2. We can design 4 point DCT first and then using this we can design an 8 point DCT and so on up to 32 [5].

The DCT obtained using the above architecture is a one dimensional DCT.

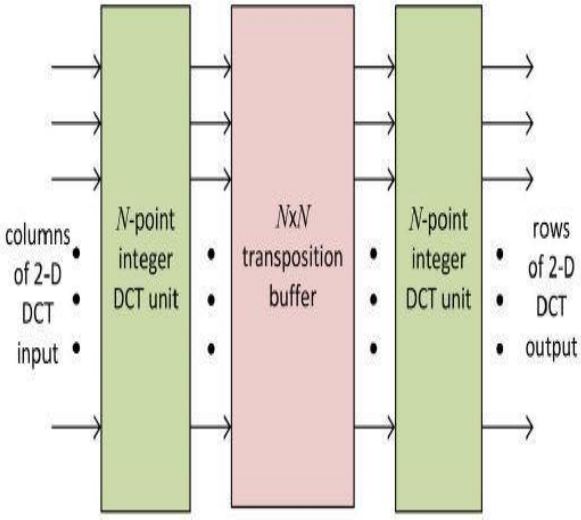

Fig. 3 Full parallel 2D DCT architecture

This obtained DCT is then transposed using a transpose matrix and go through one more DCT transform using the above structure shown in figure 2 to make it 2D DCT. The architecture for 2D DCT is given in Fig. 3.

The obtained 2D DCT using this efficient reusable architecture will have to use a lot of adders in order to reduce multipliers. Thus the chance of great power consumption due to carry propagation is high. The adders can be replaced by ETA.

The block diagram for accurate part and inaccurate is shown in figure 4 and 5 respectively. It shows that the accurate part is a conventional adder to perform simple addition in the MSB part and the inaccurate part consist of a control block and a carry-free addition block. The control block determines the mode of addition to be operated in the carry-free addition block.

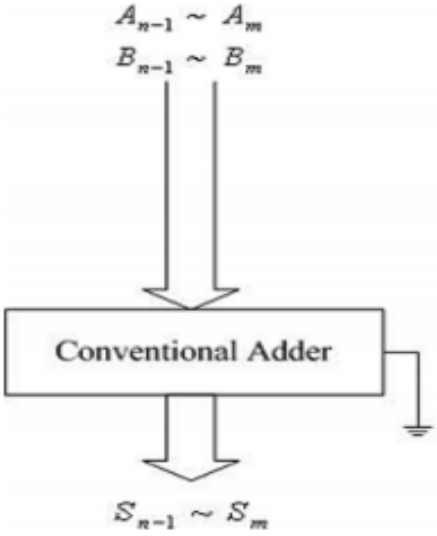

Fig: 4 block diagram of accurate part

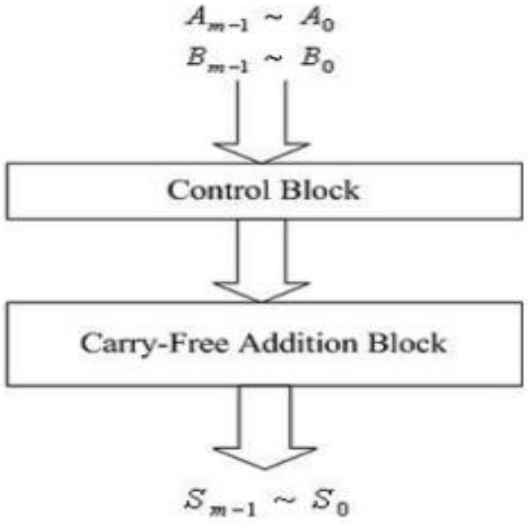

Fig: 5 block diagram of inaccurate part.

The hardware implementation of carry-free addition block is shown in figure 6. It consists of modified XOR block. Number of modified XOR blocks depends on the number of bit using in inaccurate part.

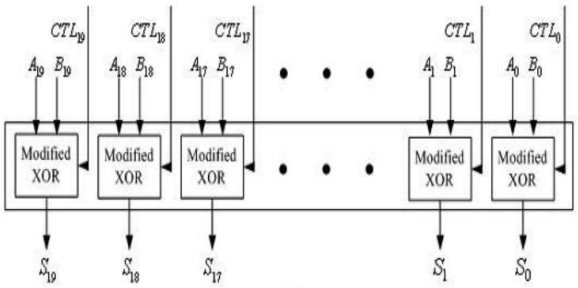

Fig: 6 design of carry-free addition block

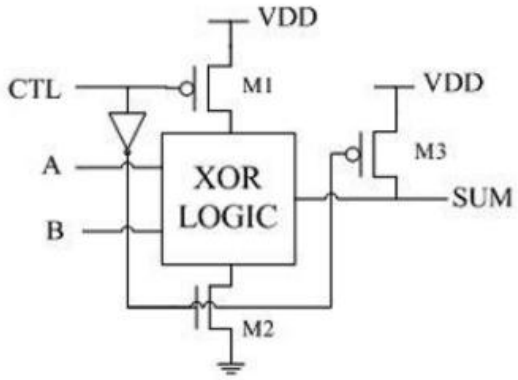

Fig: 7 design of modified XOR block

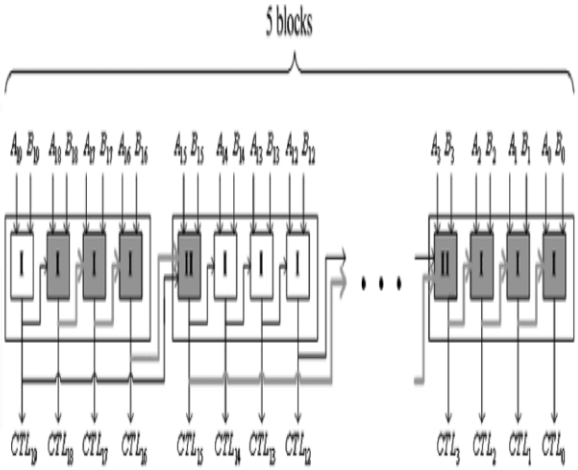

Fig: 8 design of control block.

So, for 20 bits at inaccurate part means 20 modified XOR blocks. Figure 7 gives the design of modified XOR block. The hardware implementation of control block is shown in figure 8. The comparison between the conventional adders obtained from the references and the error-tolerant added is done. The ETA is designed using Verilog HDL and simulated using Xilinx and the obtained power and area is charted in the below table 1. It provide a power efficiency up to 66.29% and an area efficiency up to 75.21%

TABLE:1 COMPARISON BETWEEN CONVENTIONAL ADDER AND ETA

Type of adder	Power (mW)	Transistor count
RCA	0.22	896
CSK	0.46	1728
CSL	0.60	2176
CLA	0.51	2208
ETA	0.13	1006

IV. CONCLUSION

Briefly in this paper, a review on an efficient and reusable architecture for DCT transform of all TU sizes is discussed. This novel discussed algorithm can be designed using any HDL language either VHDL or VERILOG HDL and can be simulated using Xilinx. Further we can implement this on FPGA. This efficient ETA structure can be implemented in this DCT to reduce power and area consumption. This technique can be used in HEVC for improved efficient data compression.

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