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Designing and Performance Evaluation of two stage CMOS OP-AMP Using 45nm CMOS Technology

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***Abstract*— This paper presents a design of two stage CMOS Operational amplifier. Operational amplifier is designed using 45nm CMOS technology. With the addition of suitable external feedback components, the modern day operational amplifier can be used for a variety of applications such as ac and dc signal amplifications, active filters, oscillators, comparators, regulators and others .In this paper we have calculated the parameters of two stage CMOS Operational amplifier like Slew rate,Gain ,Power Dissipation, and noise on different voltages and with this we have shown the effect of voltage variation on the parameters of operational amplifier. Design and Simulation has been carried on Cadence Virtuoso 6.1 tool**

***Index Terms*— OPAMP, Topologies, Gain, Slew Rate, Power Dissipation.**

I. INTRODUCTION

Operational amplifier is the most common building block of most of the electronic systems. Operational amplifier was initially designed for mathematical operations such as addition ,multiplication, subtraction, integration and hence it got its name from its original use of mathematical operations[1] .Operational amplifier is basically a high gain Differential Amplifier .There are many topologies available for operational amplifier and 2 stage operational amplifier is one among those topologies[2] . This topology uses 2 stages in cascade. In this topology gain of first stage is not significant and therefore second stage (common source) is added in cascade with the first stage to enhance the gain of the first stage and we get the significantly amplified output in the end.

Operational amplifier can be designed using cascode topologies like telescopic cascode and folded cascode topologies [3].Operational amplifier designed using telescopic cascode topologies have highest power efficiency due to its load compensation in comparison to other topologies and operational amplifier designed using folded cascade topology provides high voltage swing as compare to telescopic cascode topology[3]. Operational amplifier gain can be enhanced by using current buffer with it [4] .Operational amplifiers can be designed at low voltages by using rail to rail input / output topology [5]. Operational amplifier uses a variety of compensation techniques to increase the stability in closed loop. Miller compensation technique is one of the compensation techniques used to increase the stability of closed loop operational amplifiers [6]. Operational amplifier can be used to realize analog to digital converters, filters, comparators, oscillators, integrators, and others[7-12].

Gain and Slew rate of operational amplifier can be enhanced by using Body bias technique and Darlington pair internal biasing techniques respectively[13-14].Power dissipation in Operational amplifier can be reduced by using transistor gating technique[15]. EMI interference is very important issue for the operation of operational amplifier because if the amplitude of EMI signals increased it can damage the OPAMP IC. so to overcome this problem highly resistant CMOS operational amplifiers are designed[16].OPAMP can also be used to realize Choper Amplifiers[17].

Earlier two stage CMOS Operational amplifiers were designed using 0.5micron, 0.35 micron, 0.18 micron CMOS technologies [18-19].In this paper design of two stage OPAMP is presented at 45nm CMOS Technology.

II. CONVENTIONAL TWO STAGE OPERATIONAL AMPLIFIER

The first block is the differential amplifier in which inputs are applied at the inverting and noninverting terminals of Operational amplifier and we get a differential output which depends upon the differential input only. Second block converts the differential output generated from the first block into single ended output. The single ended output generated from the differential amplifier is not sufficiently amplified so third block in common source configuration is used to provide extra gain for the single ended output coming from the differential amplifier and with this we get sufficiently amplified output. Another block is the biasing circuitry which keeps all the MOSFETS in saturation region and this is done because MOSFET behave as an amplifier in saturation region. compensation circuitry block provides the

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stability to Operational amplifier by reducing the gain at high frequencies when negative feedback is applied to it.

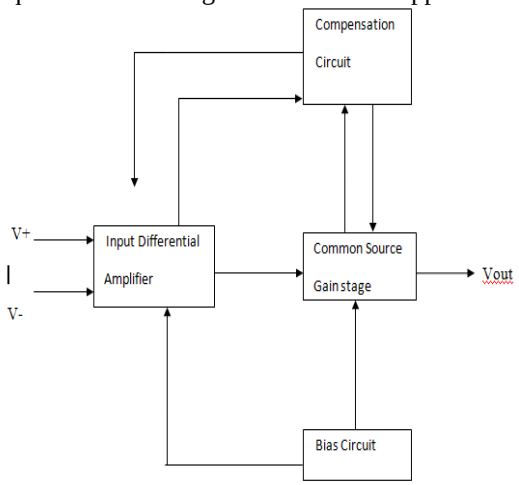

Figure 1. Block Diagram of Conventional Two stage OPAMP.

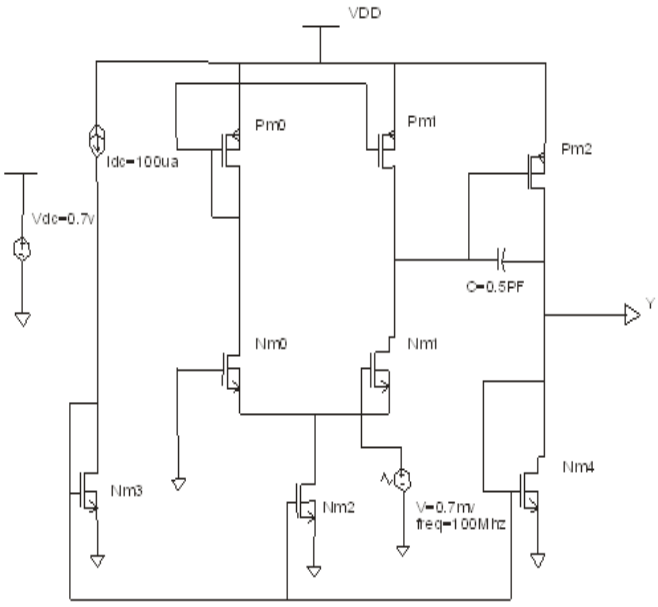

Figure 2. Schematic Diagram of Two stage OPAMP.

III. Circuit Description

The circuit Diagram of 2 stage CMOS operational amplifier consist of three sections, namely differential gain stage ,common source gain stage and biasing circuit. Now we will discuss these three stages in detail.

A. *Differential Gain stage*

Transistors NM0, NM1, PM0 and PM1 forms the first stage of operational amplifier, the differential amplifier with differential to Single ended conversion. Transistor NM0 and NM1 are the NMOS transistors with gate terminal of NM0 transistor acting as a inverting terminal of operational amplifier and gate terminal of NM1 transistor acting as a non inverting terminal of operational amplifier . Transistors NM0 and NM1 form a basic differential amplifier which will give the differential output . PMOS transistors PM0 and PM1 forms a active current mirror load for the basic differential amplifier which converts the differential output of differential amplifier into a single ended output. This topology also helps in common mode rejection ratio.

B. *Common source Gain Stage*

NMOS Transistor NM4 and PMOS transistor PM2 in common source configuration forms a second gain stage of 2 stage operational amplifier. Common source configuration is used because it provides a large gain. Amplified output of differential amplifier is obtained at the drain terminal of NM1 transistor which goes as the input to gate terminal of PM2

Transistor Transistor PM2 amplifies the signal coming as the input to its gate terminal and finally amplified output is seen across NMOS Transistor NM4.Transistor NM4 is serving as a load resistance for PM2.

C. *Biasing Circuit*

Reference current source with diode connected NMOS Transistor NM3 forms a biasing circuit of 2 stage operational amplifier. Transistor NM3 will act as a current mirror .NMOS Transistor NM2 and NM4 will draw a current depending upon there gate to source voltage which is controlled by biasing circuit.

IV. Design Procedure

Design equations are mentioned as below.

1. Slew rate = Idc/Cc, where Idc is current source and Cc is coupling capacitance.
2. First Gain stage (Av1) = -gm1/(gds2+gds4)
3. Second Gain stage(Av2) = -gm6/(gds6+gds7)
4. Gain Bandwidth Product = -gm1/Cc
5. VDS (sat) = $\sqrt{(2Ids/\beta)}$
6. Output Pole = -gm1/CL
7. RHP Zero = gm6/Cc
8. From the above relationship it is assumed that all transistors are in saturation and that Gm1=Gm2=GmI, Gm6=GmII where GmI is transconductance of first gain stage and GmII is transconductance of second gain stage.

V. Simulation Result

Table 1. Comparative Study of Operational Amplifier parameters at different voltages.

Parameters of OPAMP	Voltages for two stage OPAMP.		
	0.7 volts	0.5 volts	0.2volts
Amplified magnitude	1.011volts	1.00volts	0.932volts
Open loop Gain	40db	19db	17db

Slew Rate	7.25E6uv/sec	1.298E6uv/sec	148.7E3uv/sec
Noise	5.38517E-11	4.95691E-11	3.63397E-11
Power Dissipation	100.7uwatts	97.78uwatts	88.31uwatts

Transient Analysis:

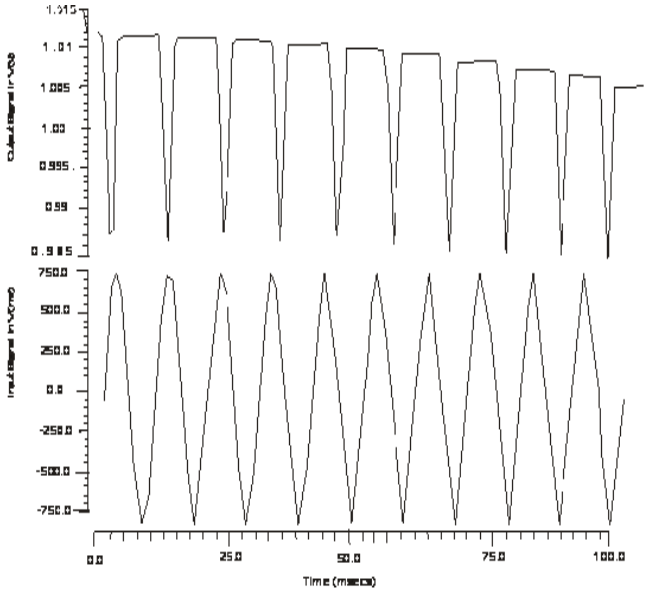

Figure 3. Input and Output waveform of two stage OPAMP.

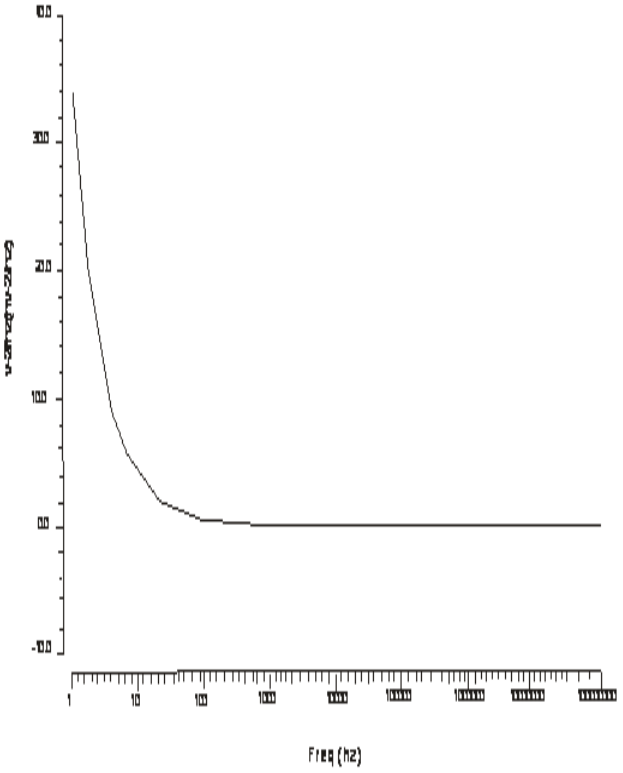

Figure 4: Noise waveform in two stage OPAMP.

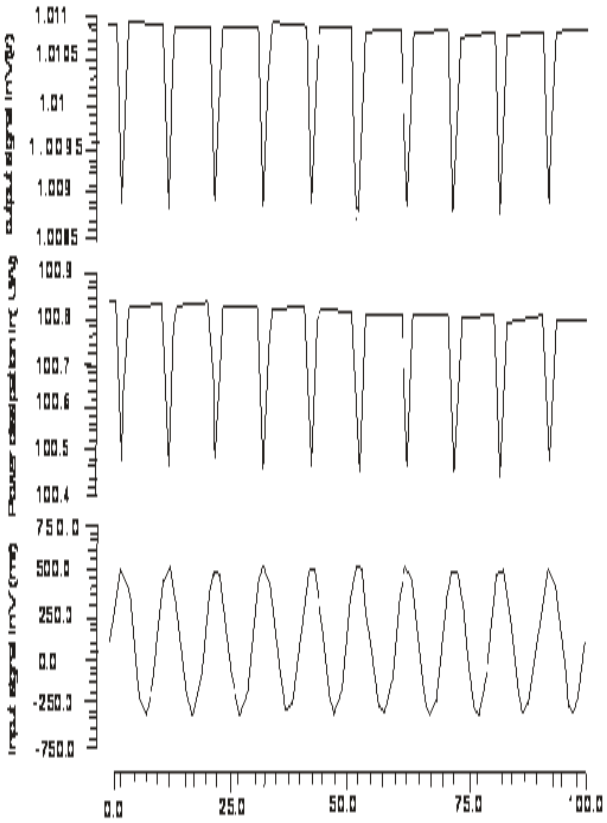

Figure. 5: Power dissipation waveform in OPAMP.

VI. CONCLUSION

Table of operational amplifier parameters at different voltages is presented in this paper. From the table it is concluded that the parameters of operational amplifier like power dissipation, noise, open loop gain and slew rate changes significantly with voltage variation. From the table it can be observed that for low noise and low power dissipation in operational amplifier, it is required to be operated at lower voltage supply while for higher gain and higher slew rate in operational amplifier it is required to be operated at higher voltage supply. Simulation results show that Gain of 40 **db** and slew rate of **7.25 v/usec** is obtained for two stage operational amplifier at 0.7 volt supply.

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