ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 6, June 2017

Low Power Approach of Clock Gating in Synchronous System like FIFO: A Novel Clock Gating Approach and Comparative Analysis

Yamini verma[1], Ravi Tiwari[2]

Abstract- A new technique of clock gating is presented to reduce dynamic power consumption. This new clock gating technique is applied on a synchronous design. Here the synchronous design is FIFO (First -in -First-out). With the help of clock gating method unwanted switching activities can be reduced. Mainly Tri-state Buffer is used to design this new low power approach. The RTL schematic of FIFO without clock gating and with new clock gating approach is also generated for implementation in hardware. Dynamic power, leakage power and total power are calculated at different voltages, frequencies and temperatures for analysis purposes. Voltage of 1.14v, 1.2v and 1.26v, frequency of 5GHz, 7GHz and 10GHz, and temperature of 25˚C and 50˚C are used for analysis. Verilog HDL has been used to implement the design. 90nm Spartan3 FPGA is used for simulation purpose. RTL implementation has been done using Xillinx ISE suite 14.2. X-POWER analyser is used for power analysis.

Index terms- clock gating, power optimization, FIFO, Tri- state Buffer, dynamic power, low power.

I. INTRODUCTION

In present scenario, semiconductor technology is increasing continuously. Packing density become higher and higher, and circuit become faster that increases power consumption and power dissipation, which is undesirable. The main task of VLSI engineers is to reduce this drawback by using energy efficient designs.

Power dissipation has a static component coming from the leakage of inactive devices and a dynamic component coming from the switching of active devices [2]. There are various types of power dissipation in a VLSI circuit. Various types of dynamic and leakage power are also present in VLSI circuit. There is various types of power saving techniques, given in reference [1]. This paper deals with only dynamic power dissipation; its task is to reduce dynamic power only.

Most components are currently fabricated using CMOS technology. In CMOS technology dynamic power is the main source of power dissipation dynamic power dissipation due to capacitive switching in digital design is given by

$$P_{dynamic} = C\ f\ VDD\hat{}2$$

Where, C is the switching capacitance, f is the clock frequency and VDD is supply voltage. By reducing any of these three variables in this equation, dynamic power can be reduced [9].

Various techniques are available to reduce dynamic power. In this paper clock gating technique is used to reduce dynamic power. It has been proved that clock signal consumes a high dynamic power as the clock net has one of the highest switching densities [5].

This paper organized as follows. Literature review is given in section 2. Section 3 deals with basics of clock gating. Proposed methodology is given in section 4. Section 5 provides the simulation result. Spartan3, 90nm FPGA is used to verify the performance of the proposed technique. Finally conclusion is provided in section 6.

II. LITERATURE REVIEW

From reference [1], it is analyzed that, there are conventionally two types of power dissipation in VLSI circuits, one is static power and other is dynamic power dissipation. Dynamic power dissipation has two components, one is switching power due to charging and discharging of load capacitance and the other is short circuit power due to non zero rise and fall time of input waveforms. Leakage power is static power, which is due to various types of leakage current present in a

MOSFET. There are a number of dynamic power reduction techniques are given, clock gating is one of them. In reference [2] a new clock gated flip-flop is designed, by using this flip-flop counter and successive approximation register is designed. These designs have more power saving and less transistor count. In reference [3] five existing clock gating techniques have been tested for different inputs. AND gate based clock gating technique has excellent power saving but it has problem of glitches and hazards. NOR gated based clock gating technique has also problem of glitches and hazards. Latch based technique is used to reduce problem of hazards but glitch problem is still there. MUX based technique has complex circuit. In reference [4] timing error under transient noise is removed by applying programmable time borrowing and delayed clock gating technique. In reference [5] it is proved that clock signal consumes a high dynamic power as the clock net has one of the highest switching densities. In reference [6] the work in this paper investigates the various clock gating techniques that can be used to optimise power in VLSI circuits at RTL level and various issues involved while applying this power optimization techniques at RTL level. Reference [7] deals with latch free clock gating technique for reduction of dynamic power and clock power consumption in a benchmark circuit. Comparison is made at different frequencies with clock gating and without clock gating. It is observed from the results that power has been reduced by 73.68% and 97.06% at 10GHz and 100GHz frequency respectively. In reference [8] latch free clock gating technique is applied on CPU.

III. CLOCK GATING BASICS

Clock power is the main source of chip power dissipation. Clock gating is a low power technique; it is used for the reduction of dynamic power dissipation in a VLSI circuit. In clock gating technique clock is not directly applied to the functional unit, instead it is applied through a controlling unit. This controlling unit has a control signal, which controls the propagation of clock signal under a certain condition computed by controlling circuit. This controlling circuit is called Clock Gating circuit. The saving is mainly due to the switching capacitance reduction in the clock network and the switching activity in the logic fed by the storage elements because unnecessary transitions are not loaded when the clock is not active. Clock gating is illustrated in figure 1 block CG, which inhibits the clock signal when the idle condition is true, is associated with each sequential functional unit [6].

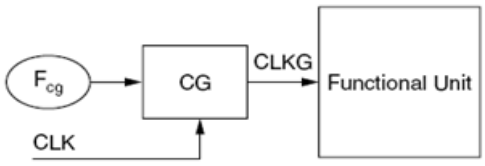

Fig 1. Clock gating principle

IV. PROPOSED METHEDOLOGY

A. Novel design of clock gating based on Buffer

In our proposed approach Tri state buffer is associated with the OR logic. There is no glitch and hazard problem, because of presence of Buffer logic. This proposed clock gating technique has small number of Gate count, so design is simple and require less area for implementation. This design works only at negative edge of clock signal.

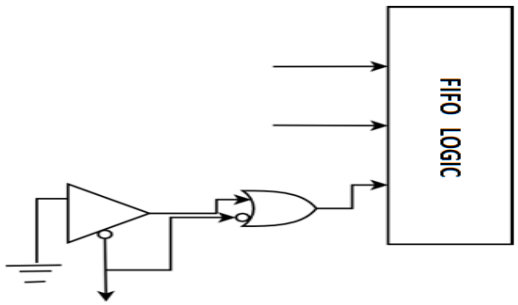

Fig. 2 proposed clock gating approach

B. FIFO (First-in-First-Out)

In computer programming, FIFO (first-in, first-out) is an approach to handling program work requests from queues or stacks so that the oldest request is handled first. In hardware it is either an

array of flops or Read/Write memory that store data given from one clock domain and on request supplies with the same data to other clock domain following the first in first out logic. The clock domain that supplies data to FIFO is often referred as WRITE OR INPUT LOGIC and the clock domain that reads data from the FIFO is often referred as READ OR OUTPUT LOGIC. FIFOs are used in designs to safely pass multi-bit data words from one clock domain to another or to control the flow of data between source and destination side sitting in the same clock domain.

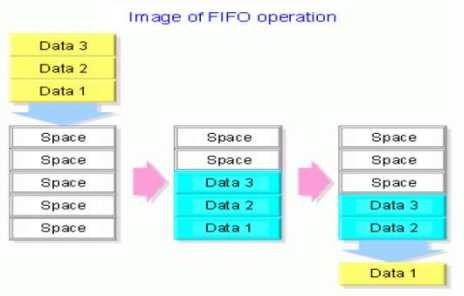

Fig. 3 Data Flow through FIFO

V. SIMULATION RESULT

A. *FIFO- without clock gating*

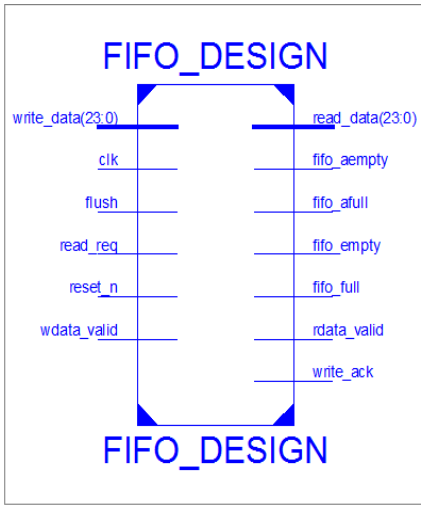

Fig. 4 Top Module of FIFO

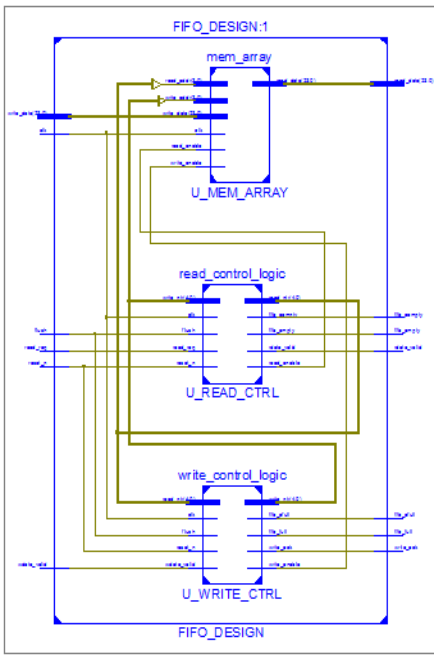

Fig. 5 RTL Schematic of FIFO

FIFO is made up of three blocks, namely, Memory, Read control logic, Write control logic.

B. *FIFO with Proposed clock gating*

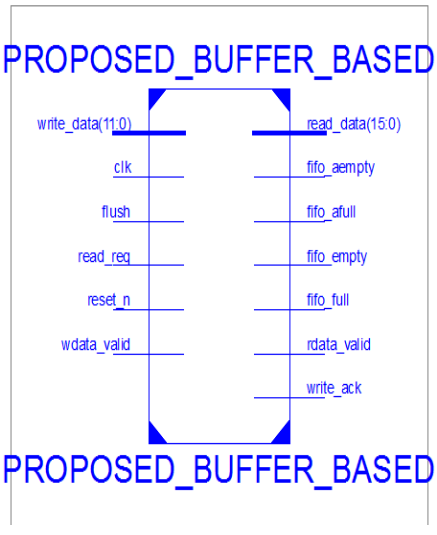

Fig. 6 Top module of FIFO with clock gating

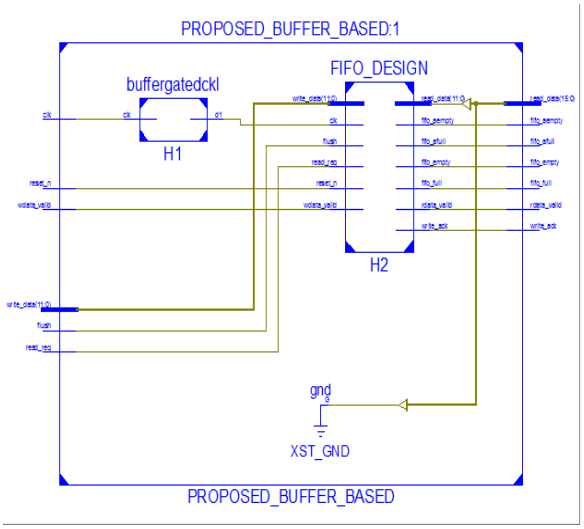

Fig. 7 RTL view of FIFO with clock gating

Table 1: Dynamic power (watt), with and without clock gating technique with different voltages and freq.=10 GHz, 25˚C

Design	1.14v	1.2v	1.26v
Without clock gating	1.115	1.125	1.274
With proposed clock gating	0.136	0.954	1.031

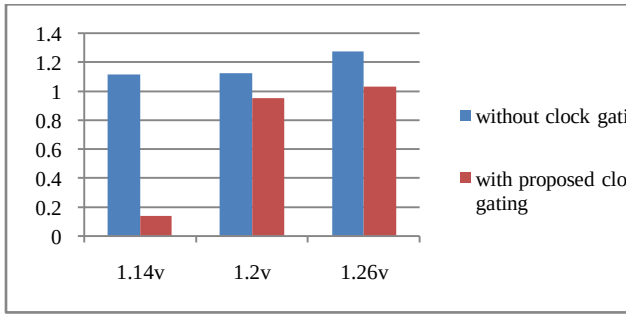

Fig. 8 Supply voltage on Y- Axis

Table 2: Dynamic power (watt), with and without clock gating technique with different frequency and V= 1.2v, 25˚C

Design	5GHz	7GHz	10GHz
Without clock gating	0.697	0.986	1.125
With proposed clock gating	0.613	0.778	0.831

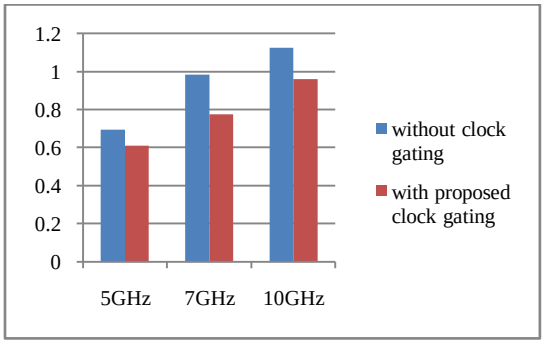

Fig. 9 Supply voltage on Y-Axis

Table 3: Dynamic power (watt) with and without clock gating technique with different temperature and V= 1.2v, freq.= 10GHz

Design	25˚C	50˚C
Without clock gating	0.401	1.247
With proposed clock gating	0.170	1.036

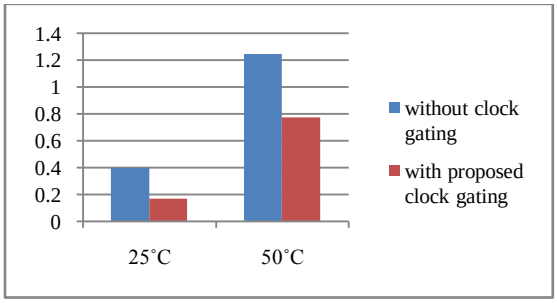

Fig. 10 Supply voltage on Y-Axis

VI. CONCLUSION

This paper presents a proposed clock gating technique, which is applied on synchronous system like FIFO. Power has been calculated without clock gating technique and with proposed clock gating technique applied to FIFO. Power is calculated at different voltages, frequency and temperature for analysis purpose. It is concluded that dynamic power reduces after the application of clock gating technique but static power is approximately independent of clock gating technique. After application of clock gating technique in FIFO there is

small amount of reduction of power at lower frequency, but as clock frequency increases, reduction of dynamic power become high, at 7GHz reduction of dynamic power is only 21.09% but for higher frequency like 10GHz dynamic power reduction become 26.13%. It has been seen that when temperature changes, there is small change in dynamic power but static power changes.

So, the proposed clock gating technique is effective in reduction of power.

ACKNOWLEDGEMENT

The author would like to thank Prof. Mr. Ravi Tiwari and Director SSGI, Bhilai for their research, motivation and support.

REFERENCES

[1] Paul, Bipul C., Amit Agarwal, and Kaushik Roy. "Low-power design techniques for scaled technologies." INTEGRATION, the VLSI journal 39.2 (2006): 64-89.

[2] Shaker, Mohamed O., and Magdy Bayoumi. "A clock gated flip-flop for low power applications in 90 nm CMOS." Circuits and Systems (ISCAS), 2011 IEEE International Symposium on. IEEE, 2011.

[3] Kathuria, J. ; Ayoubkhan, M. ; Noor, A. ; ―A Review of Clock Gating Techniquesl, MIT International Journal of Electronics and Communication Engineering, August 2011, vol.1 no.2 , pp 106-114.

[4] Chae, Kwanyeob, and Saibal Mukhopadhyay. "Resilient Pipeline Under Supply Noise With Programmable Time Borrowing and Delayed Clock Gating." Circuits and Systems II: Express Briefs, IEEE Transactions on 61.3 (2014): 173-177.

[5] H. Kawaguchi and T. Sakurai, 'A reduced clock-swing flip-flop (RCSFF) for 63% power reduction,' IEEE J. Solid-State Circuits, vol.33, pp. 807-811, May. 1998.

[6] Shinde, Jitesh, and S. S. Salankar. "Clock gating—A power optimizing technique for VLSI circuits." India Conference (INDICON), 2011 Annual IEEE. IEEE, 2011.

[7] Tomar, Beer Pratap Singh, et al. "Power Reduction of ITC'99-b01 Benchmark Circuit Using Clock Gating Technique." Computational Intelligence and Communication Networks (CICN), 2013 5th International Conference on. IEEE, 2013.

[8] Sulaiman, Diary Rawoof. "Using clock gating technique for energy reduction in portable computers." Computer and Communication Engineering, 2008. ICCCE 2008. International Conference on. IEEE, 2008.

[9] Sahni, Kanika, et al. "Power Optimization of Communication System Using Clock Gating Technique." Advanced Computing & Communication Technologies (ACCT), 2015 Fifth International Conference on. IEEE, 2015.

[10] Zhang, Yan, Jussi Roivainen, and Aarne Mämmelä. "Clock-gating in FPGAs: A novel and comparative evaluation." Digital System Design: Architectures, Methods and Tools, 2006. DSD 2006. 9th EUROMICRO Conference on. IEEE, 2006.

[11] Li, Hai, et al. "Deterministic clock gating for microprocessor power reduction."High-Performance Computer Architecture, 2003. HPCA-9 2003. Proceedings. The Ninth International Symposium on. IEEE, 2003.

Yamini Verma PG Student [VLSI], Dept. of ECE, ShriShankracharya Group of Institution, Bhilai, Chhattisgarh, India

Ravi Tiwari Assistant professor, Dept. of ECE, ShriShankracharya Group of Institution, Bhilai, Chhattisgarh, India