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Analysis and Performance Comparison of Different SRAM Cells

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Abstract: SRAM plays an important role in sequential circuits where a memory element is needed. As bulky memory chips needs several SRAM cells, the power associated with each SRAM cell is a major factor to be considered. This project proposes a new architecture of SRAM which consumes low power when compared to the conventional SRAM. Here different SRAM cells are implemented and comparison of results in the presence of different metrics like power, delay and number of transistors are provided. Here the pre-layout and post-layout simulations are done in 130nm CMOS technology.

Index Terms – Leakage current, low power, SRAM, System on chip (Soc), D-latch.

I. INTRODUCTION

By using a new model called VAR-TX (D2D (die 2 die) and WID (with in die). 6T SRAM cell can be designed in 16 nm technology. Threshold voltage (V_{TH}), Gate length (L), and Supply voltage (VDD) are varied to increase the performance and energy efficiency of the system [7]. To increase the performance of SRAM the design challenges and techniques are using End of Scaling methods in CMOS technology. This impacts on technology scaling, such as signal loss due to leakage, degradation of noise margin due to V_T scatter caused by process variations and random dopant fluctuation [6]. An asymmetrical write assist cell virtual ground biasing scheme and positive feedback sensing keeper schemes are used to improve the read static noise margin, write margin and operation speed of a single ended read/write 8T SRAM cell. This 8T SRAM cell is implemented by using 90 nm CMOS technology [5]. A new bit-interleaving 12T sub threshold SRAM cell with Data-Aware Power-Cut-off (DAPC) Write assist to improve the write ability to mitigate increased device variations at lower supply voltage. The 12T SRAM cell is demonstrated by a 4KB SRAM macro implemented in 40nm CMOS technology [4]. In order to avoid the limitations of 6T SRAM bit cell in

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term of minimum supply voltage, $V_{DD\ MN}$. A new technique of sub threshold 10T SRAM bit cell with read/write selection is implemented using 28 nm CMOS technology [3]. Leakage power, especially sub threshold leakage and gate leakage and soft error are challenging the design of SRAM. In order to simultaneously decrease in leakage power and enhances the resistance to soft error, a low leakage robust SRAM is designed using Hybrid SRAM (HSRAM) cell in HSPICE and ISE 8.0 [2]. 5T SRAM cell is designed to decrease the bit line leakage to improve read/write performances and to decrease the power dissipation. In this paper D-Latch is designed by using 5T SRAM cell in 130nm CMOS technology is implemented and results are presented [1].

II. METHODOLOGY

The design of SRAM can be implemented by using different software tools like Cadence, Mentor Graphics Tool, Matlab, and Xilinx. If the design is implemented using Matlab or Xilinx, it is difficult to connect the components through coding. Mentor Graphics Tool makes it easy, simply by performing the design from the transistor level. In this tool the pre-layout simulation can be performed after the design of circuit. Different parameters are analysed by using measurement tool. Post-layout simulation produces the waveforms after the addition of parasitic components like RLC (Resistor, Inductor, and Capacitor).

III.PROPOSED TECHQNIQUE

5T SRAM CELL

The below figure shows 5T SRAM cell in order to store a single bit memory either 1 or 0.When compared to conventional 6T SRAM,5T SRAM avoids the use of one of the write line transistor at BLB side, only single write line transistor is connected to the back to back inverter. During 'Write' operation WL is made 1, which makes the transistor M5 to ON condition. As a result the bit which is assigned on bit line stores at node Q through transistor M5. During 'Read' operation WL line is asserted. If previous write operation performed with storage of bit1, then M4 and M6 tends to become ON. So VDD directly appears on BL line through M6 and M5.If bit 0 is stored during previous write operation, this makes M2 and M1 to become ON.As a result VDD appears on BLB line through M2 [9].

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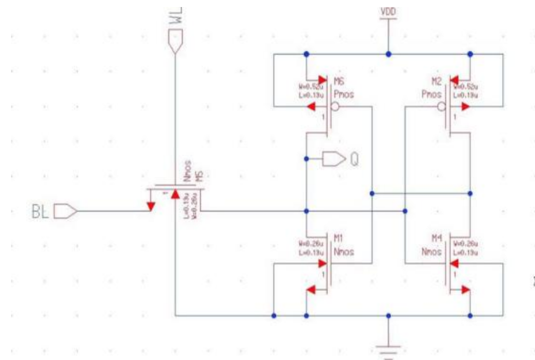

Figure 1: Proposed 5T SRAM Schematic.

SRAM is used in cache memory of a computer or as part of the RAM digital to analog converter on a video card. Static Random Access Memory (SRAM) is also used for high-speed registers, caches and small memory banks like a frame buffer on a display adapter. Several scientific and industrial subsystems, modern appliances, automotive electronics, electronic toys, mobile phones, synthesizers and digital cameras also use SRAM. It is also highly recommended for use in PCs, peripheral equipment, printers, LCD screens, hard disk buffers, router buffers and buffers in CDROM / CDRW drives.

A. D-LATCH USING 6T SRAM CELL

The belowfigure shows D-Latch 6T Based SRAM cell, which is used to store single bit binary data 1 or 0. It consists of 2 word line transistors in 6T SRAM. The output of SRAM cell is connected to D_{in} of D-Latch. During the 'write' operation WL is made high, as a result the input BL which is given to SRAM cell directly stored in the D-Latch for a positive clock cycle. During the 'read' operation WL is made low. The data which is stored during write operation appears at the output port D-Latch during the positive clock.

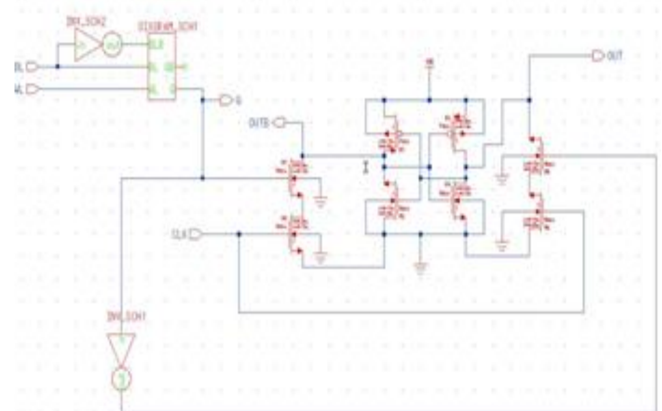

Figure 2: D Latch using 6T SRAM Schematic.

B. D-LATCH USING 5T SRAM CELL

The below figure shows D-Latch 5T Based SRAM cell, which is used to store single bit binary data 1 or 0. As it avoids the use of write line transistor at BLB side, the output (Q) is connected to input port of D-Latch. The operational behaviour of D-Latch entirely depends on clock signal.

As D-Latch is implemented using gated SR flip-flop, the output of D-Latch depends on set-reset conditions. The outputs from SRAM cell will have effect on the output of D-Latch only during the positive clock edge.

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During the write operation WL is made high, as a result the input BL which is given to SRAM cell directly stored in the D-Latch for a positive clock cycle.

During the read operation WL is made low. The data which is stored during write operation appears at the output port D-Latch during the positive clock.

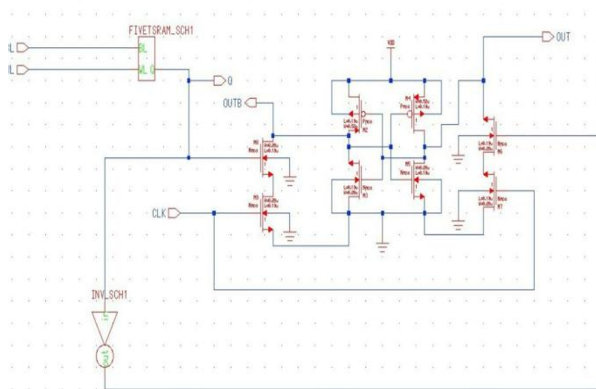

Figure 3: D Latch using 5T SRAM Schematic.

IV.SIMULATION RESULTS

The below figure shows the pre-layout simulation of 5T SRAM cell. The 8 bit input of 11000000 is given at BL input. The WL line is assigned with pattern of 10101010.When WL is made high (i.e. 1).The corresponding input at BL port (i.e.1) is written into the SRAM cell at 'Q' port. During read operation (i.e. when WL=0) the data which was written during previous write operation is read out from SRAM cell through port 'Q'.

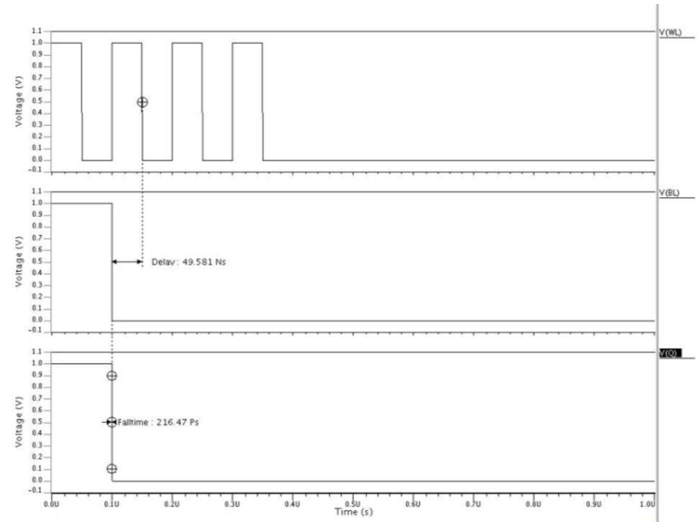

Figure 4: Proposed 5T SRAM Cell Pre-Layout Simulation.

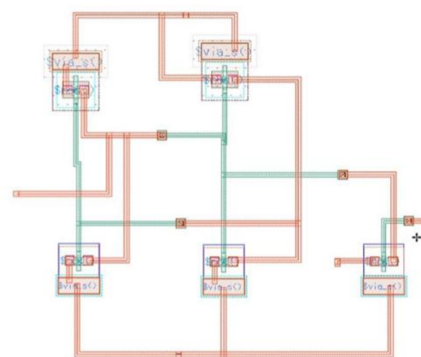

Figure 5: Proposed 5T SRAM Layout.

Table (1) shows the comparison between, conventional 6T, 8T, ST 11T &5T SRAM Cells on the basis of different metrics in the Pre-Layout Simulation.

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S.No	PARAMETER	LOGIC			
		CONVENTIONAL 6T SRAM CELL	8T SRAM CELL	11T SRAM CELL	PROPOSED5T SRAM CELL
1	POWER DISSIPIATION	1.2441 nW	1.3168 nW	3.4736 nW	1.2421 nW
2	DELAY	50.265 nS	49.985 nS	384.00 pS	50.462 nS
3	NUMBER OF TRANSISTORS	6	8	11	5

Table (1) Comparison between different SRAM Cells in pre-layout simulation.

The below figure shows the pre-layout simulation of D-Latch based 6T SRAM cell. The 8 bit input of 11001000 is given at BL input. The WL line is assigned with pattern of 10101010.When WL is made high (i.e. 1).The corresponding input at BL port (i.e. 1) is written into the SRAM cell at 'Q' port. During read operation (i.e. when WL=0) the data which was written during previous write operation is read out from SRAM cell through port 'OUT'. The inverted output of 'OUT' appears at 'OUTB'. All these operations either write or read tense to appear only during positive edge of clock.

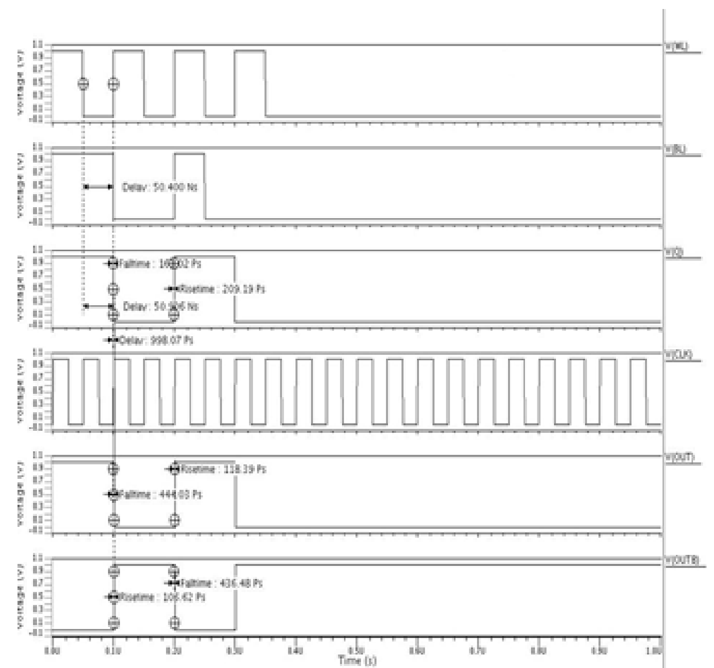

Figure 6: D-Latch Based 6T SRAM Cell Pre-Layout Simulation.

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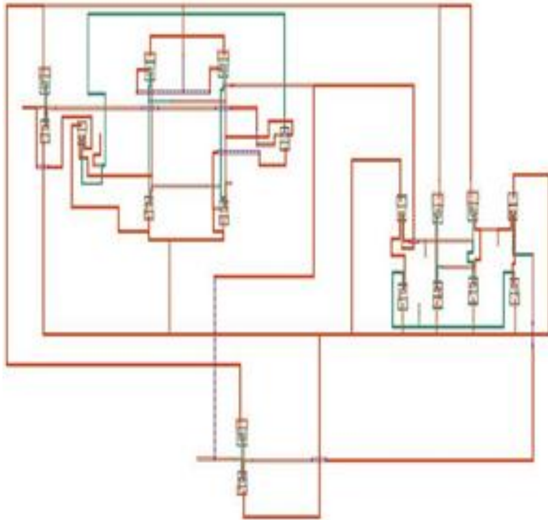

Figure 7: D-Latch Based 6T SRAM Cell Layout.

The below figure shows the pre-layout simulation of D-Latch based 5T SRAM cell. The 8 bit input of 11000000 is given at BL input. The WL line is assigned with pattern of 10101010.When WL is made high (i.e. 1).The corresponding input at BL port (i.e. 1) is written into the SRAM cell at 'Q' port. During read operation (i.e. when WL=0) the data which was written during previous write operation is read out from SRAM cell through port 'OUT'. The inverted output of 'OUT' appears at 'OUTB'. All these operations either write or read tense to appear only during positive edge of clock.

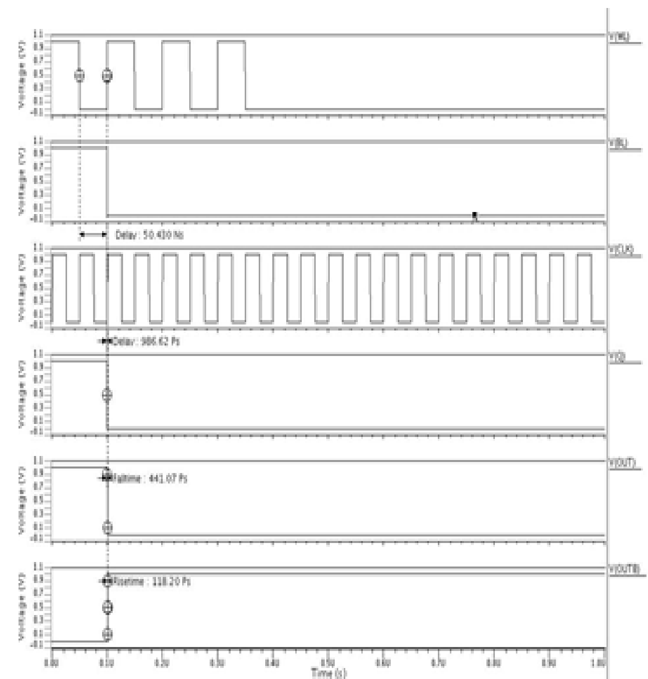

Figure 8: D-Latch Based 5T SRAM Cell Pre-Layout Simulation.

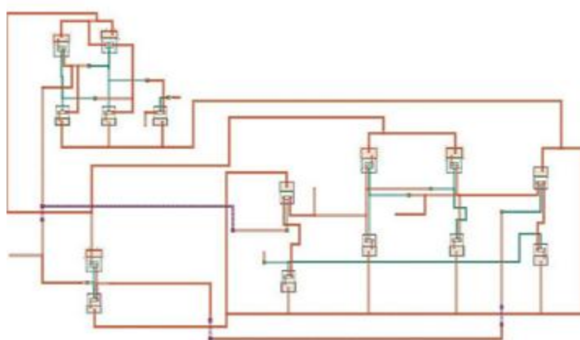

Figure 9: D-Latch Based 5T SRAM Cell Layout.

Table (2) shows the comparison between D-Latch Based 5T SRAM and D-Latch Based 6T SRAM cell on the basis of different metrics in the Pre-Layout Simulation.

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S.No	PARAMETER	LOGIC	
		D-LATCH BASED 6T SRAM	D-LATCH BASED 5T SRAM
1	POWER DISSIPATION	3.0179 nW	2.9452 nW
2	DELAY	50.906 nS	50.430 nS
3	#Tr	6	5

Table (2) Comparison between D Latch Based 6T &5T SRAM Cells in pre-layout Simulation.

CONCLUSION

A 5T SRAM cell using 130nm technology is designed. The pre-layout and post-layout simulation results are obtained. These results are compared with the conventional 6T, 8T, Schmitt trigger 11T circuit simulation results. These results prove that 5T SRAM cell is better in performance and power dissipation in both pre-layout and post-layout simulations. By using this 5T SRAM cell D-Latch using 5T SRAM cell is implemented and the pre-layout and post-layout results are compared with the D-Latch which uses the 6T SRAM. This comparison results also prove that D-Latch using 5T SRAM cell is better in performance and power dissipation in both pre-layout and post-layout simulation.

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