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A Low Power and Low Complexity Multiplier Using DPTL Logic

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ABSTRACT*–*Power, speed and area are prime design constraints for portable electronics devices and signal processing applications. Multiplier plays an important role and these are widely used in digital signal processing systems. In this paper it presents a variety of EXOR gates with reducing power consumption and acquiring low power dissipation and minimum delay. By using double pass transistor logic (DPTL) EXOR gate to design a full adder with better results. An array multiplier circuit is designed by using this full adder and it also responsible for reducing the power consumption. Simulation results are carried out using Mentor Graphics tool in 130nm technology.

INDEX TERMS*: *Multiplier, EXOR gate, DPTL logic, Mentor Graphics tools.

1. INTRODUCTION

Multipliers are one of the basic components in the design of digital communication circuits. These multipliers are fast, reliable and efficient components that are utilised to implement any operation. In the majority of digital signal processing (DSP) application the multiplier can perform the multiplication operation consists of producing partial products then adding these partial products and then final product is obtained.

The speed of the multiplier depends on the number of partial products and the speed of the adder. So the multipliers have a significant impact on the performance of the entire system. The high speed DSP's requiring both adders for addition and multipliers for multiplications.

Conventional static CMOS is a better technique for most of the processor designs [1]. Alternatively, static pass transistor circuits are suggested for low-power applications [2]. Design of high-speed low-power circuits with CMOS technology has been a major research problem for many years. Several logic families have been proposed and used to improve circuit performance beyond that of conventional static CMOS family [4].

In addition, due to technology scaling and the increasing number of transistors on chip, the performance of static CMOS circuits comes at substantial area/power dissipation costs that may be critical, especially for portable appliances. New logic families which are addresses the power and performance challenges explored [5].

The Pass-Transistor Logic (PTL) is a better way to implement circuits which are designed for low power applications. The advantage of that PTL is one pass-transistor network (either PMOS or NMOS) is sufficient to implement the logic function, which results in smaller number of transistors and smaller input load and less requirements [6].

DPL uses both PMOS and NMOS devices in the pass transistor network to avoid output swing reduction [7]. Double pass-transistor logic is shown to improve circuit performance at reduced supply voltage. Its symmetrical arrangement and double-transmission characteristics improve the gate speed without increasing the input capacitance [8].

2. EXOR GATE IMPLEMENTATION USING NAND GATES

In CMOSEXOR gate it performs modulo sum operation without including carry is known as EXOR gate. An EXOR gate is normally two input logic gate where, output is logical 1 when only one input is logical 1. When the two inputs are equal, that is two inputs are 1 or two inputs are 0, the output will be logical 0. This gate is called as EXOR or exclusive OR gate because, its output is only 1 when one of its input is exclusively 1.

Here the EXOR gate is designed by using nand gate structure. The structure of EXOR gate with nand gate is given below,

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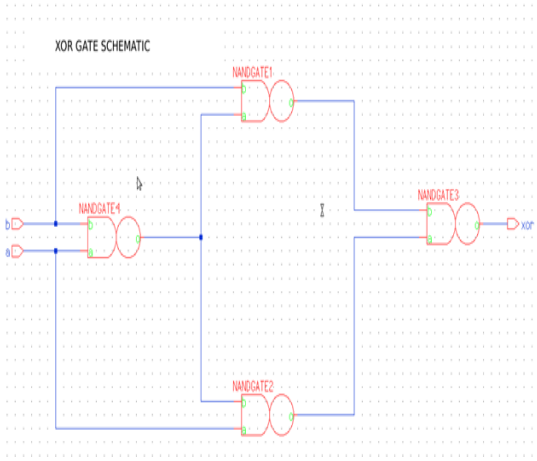

Fig 1: Schematic of two input EXOR gate by using nand gates

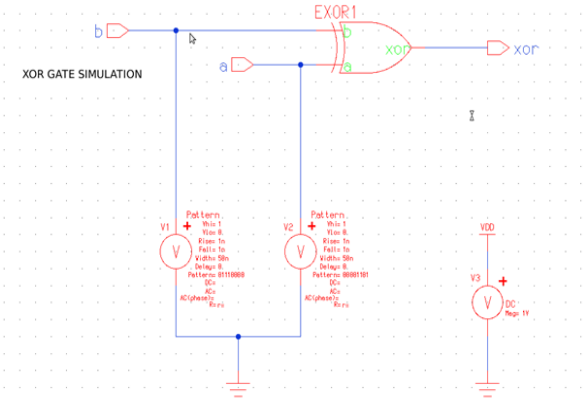

Fig 2: Simulation circuit of EXOR gate by using nand gates

After successful simulations the waveforms are implemented for the EXOR gate by using nand structure are obtained in mentor graphics tool.

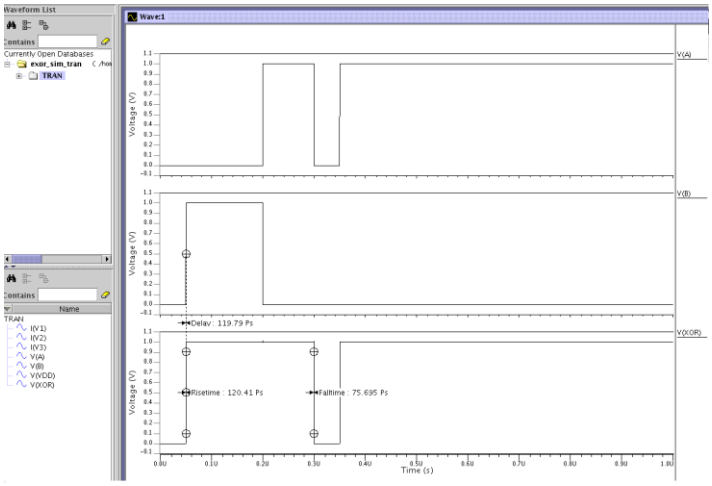

Fig 3: Simulation waveforms of EXOR gate by using nand gate

Existing EXOR gates are simulated using mentor graphics tool between the voltages of 1V to 1.2V using 130nm CMOS technology. Simulation is performed at varying supply voltages to show the effect of different voltages to the output swing of EXOR circuits. Here the transient results are shown with the voltage of 1V. Here the transient analysis is done for the circuit to know the values of rise time, fall time and delay by using measurement tool.

By using nand gates to design EXOR gate the power dissipation more because the more number of transistors are used in the designing. By this way in the designing of EXOR gate the transistor count increases automatically the power dissipation also increased.

The increasing level of device integration and the growth in complexity of microelectronic circuits, reduction of power dissipation has come to a primary design goal. While power efficiency always been a desirable measurements in electronic circuits, recently it becomes a limiting factor for broad range of applications.

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3. PROPOSED CIRCUIT OF EXOR GATE

To avoid the delay problem in CPL, a PMOS transistor has been connected in parallel with NMOS to produce a full swing like full Vdd or full ground at the output. Hence here we are using both PMOS and NMOS it is called double pass transistor logic (DPTL). To overcome the drawback of CPL, DPTL has been developed for low power applications and the advantage is either PMOS or CMOS can be used to implement the logic design. In this paper all the logic circuits has been implemented by DPTL.

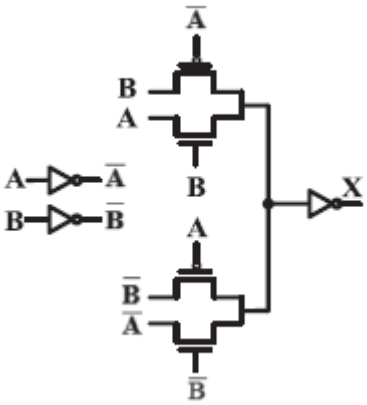


Fig 4:Structure of the double pass transistor logic (DPTL)

A Double Pass Transistor Logic (DPL) XOR gate is shown above figure this structure provides a full voltage swing because the inverter could be placed at the output node of the DPTL logic. Due to this reason it provides a full voltage swing.

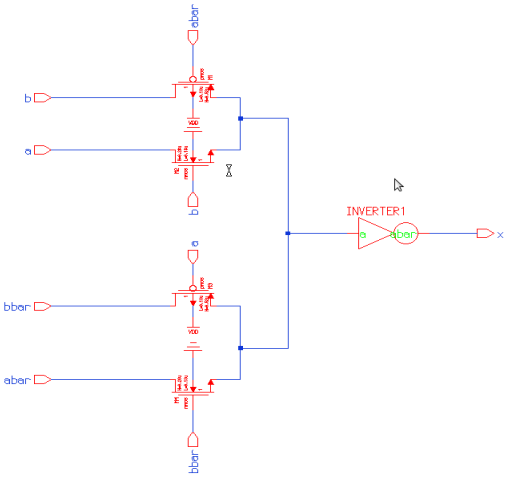


Fig 5: Schematic of the DPTL logic

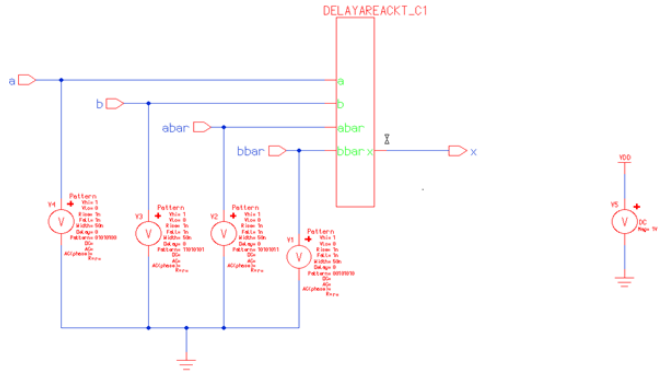


Fig 6: Simulation diagram of DPTL logic

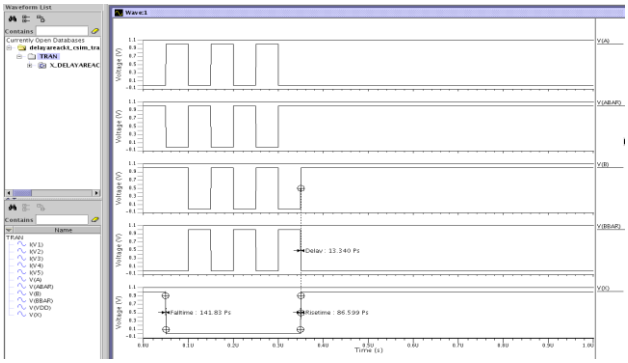


Fig 7: Simulation waveforms of DPTL Logic

4. PROPOSED ARCHITECTURE OF ARRAY MULTIPLIER

The array multiplier is a regular structure therefore speed of operation becomes simple and it occupies less area since it has small size. In VLSI, the regular structures can be fabricated one after another; this reduces the amount of mistakes and also reduces circuit complexity design. A basic multiplier can be divided into three sections partial product generation, partial products addition and final addition.

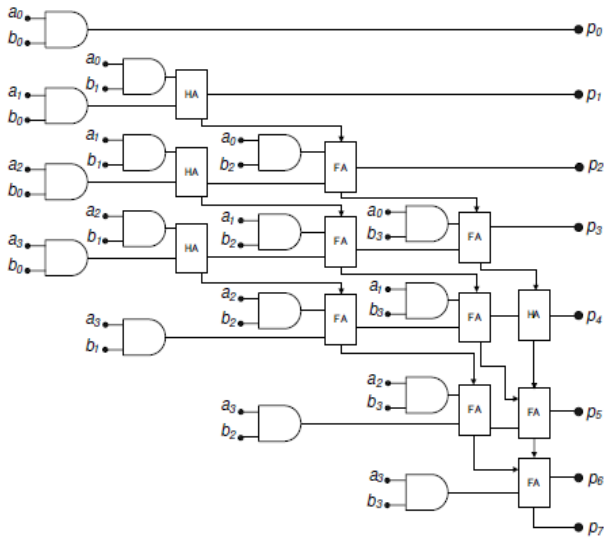


Fig 8: Architecture of 4x4 array multiplier

In this paper, an array multiplier is proposed that can produces partial product terms by using less number of transistors. The circuit is implemented using double Pass transistor logic (DPL). In nano meter scale leakage power dominates the dynamic as well as static powers due to hot electrons. So the concentration is on trade off power in array multipliers.

In the proposed array multiplier the full adder cells and half adder cells are implementing by using double pass transistor logic (DPTL).Circuit is designed using inverter based 4T XOR gates in the designed full adder cell and shows remarkable improvements in power and delay.

This full adder cell has less power consumption as it has no direct path to ground .The elimination of a path to the ground reduces power consumption. Throughput is a measure it is defined by how many multiplications can be performed in a given amount of time for a simple and combinational multiplier; throughput is a function of latency.

5. SIMULATION RESULTS OF ARRAY MULTIPLIER

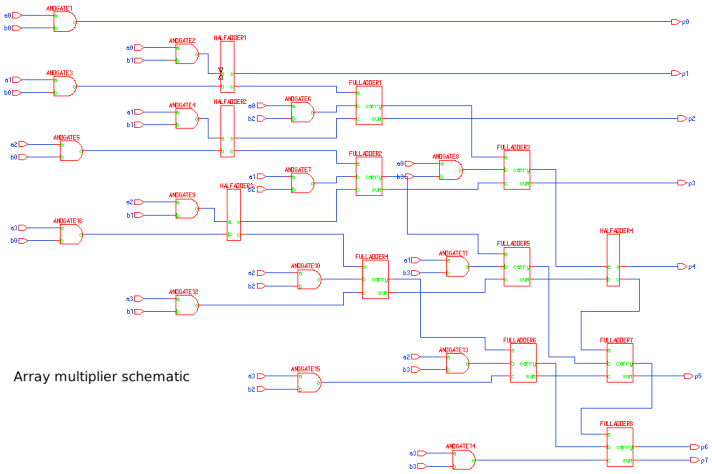


Fig 9: Schematic diagram of 4x4 array multiplier using DPTL Logic

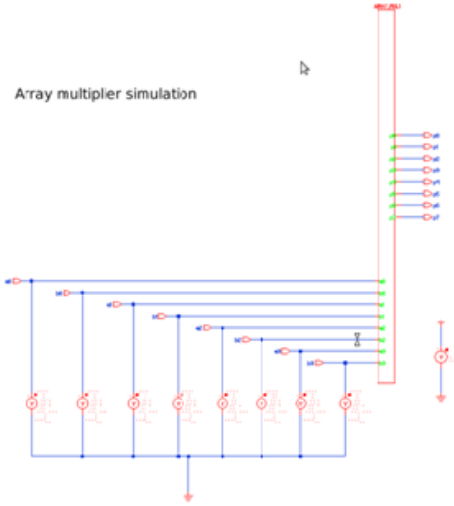


Fig 10: Simulation diagram of 4x4 array multiplier using DPTL logic

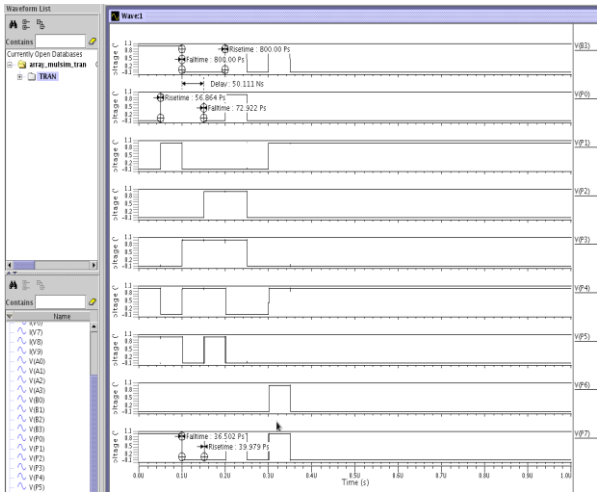
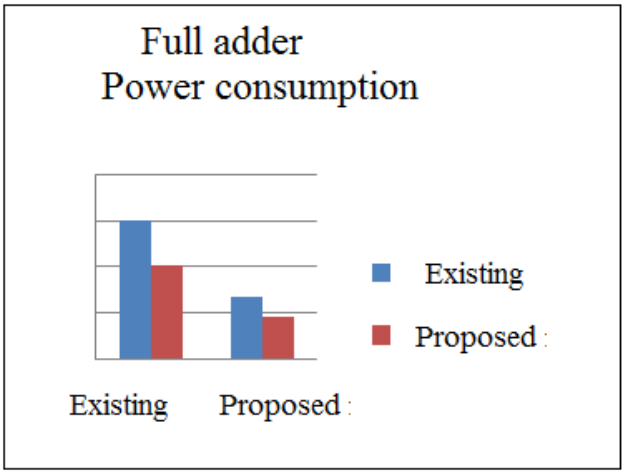
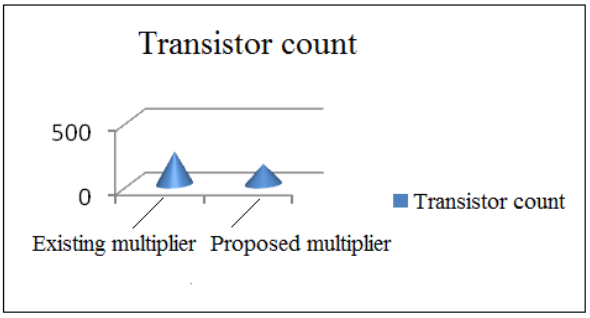


Fig 11: Simulation waveform of 4x4 multiplier using DPTL logic



6. COMPARISON DIAGRAMS



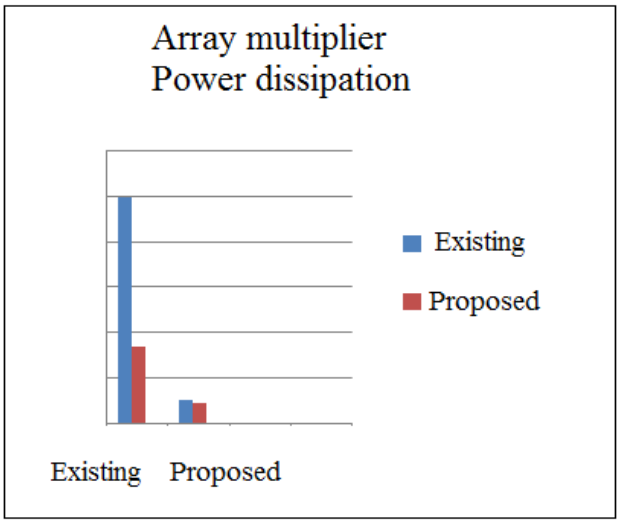
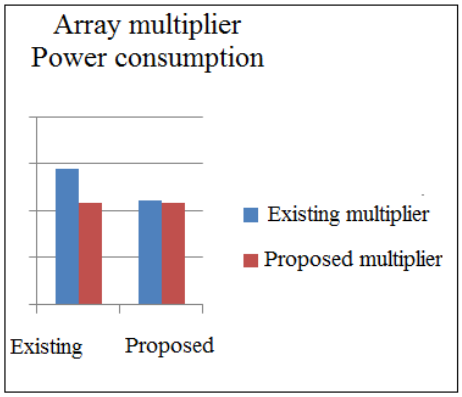


Fig 12: Power dissipation factor of array multiplier chart



7. LAYOUTS IMPLEMENTED IN MENTOR GRAPHICS 130NM TECHNOLOGY

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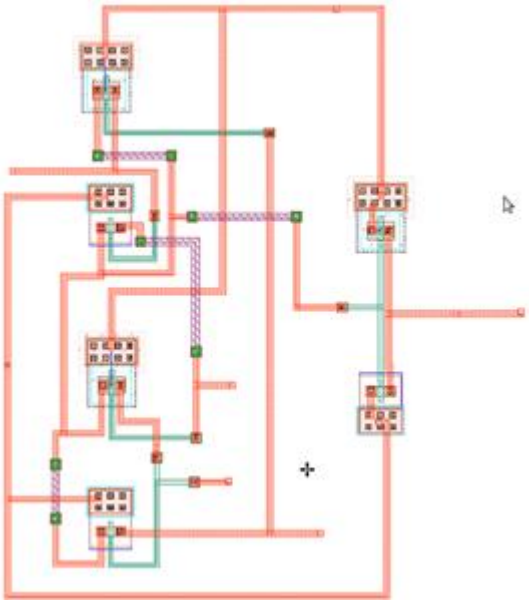

Fig 13: DPTL logic EXOR gate layout

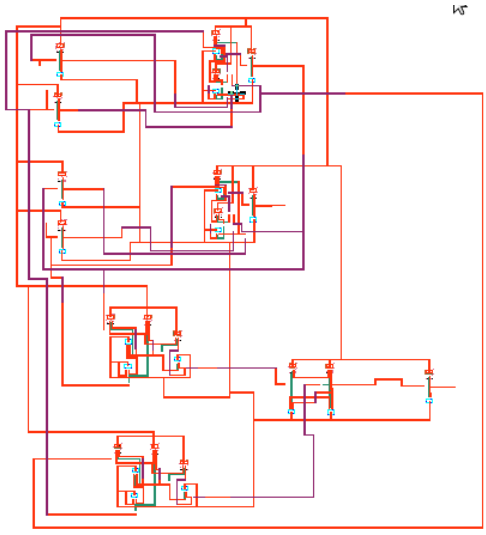

Fig 14: DPTL logic using fulladder layout

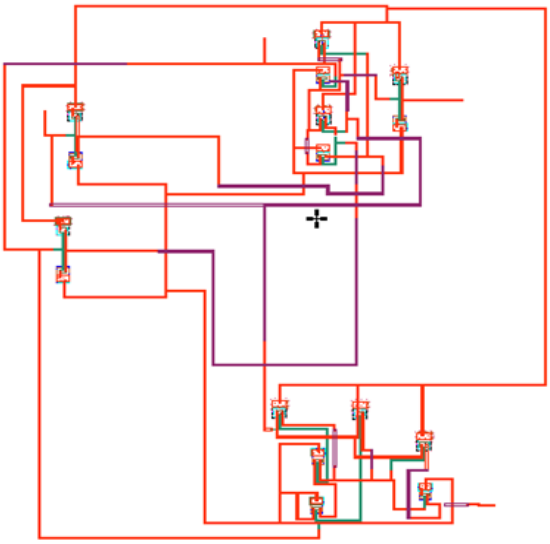

Fig 15: DPTL logic using halfadder layout

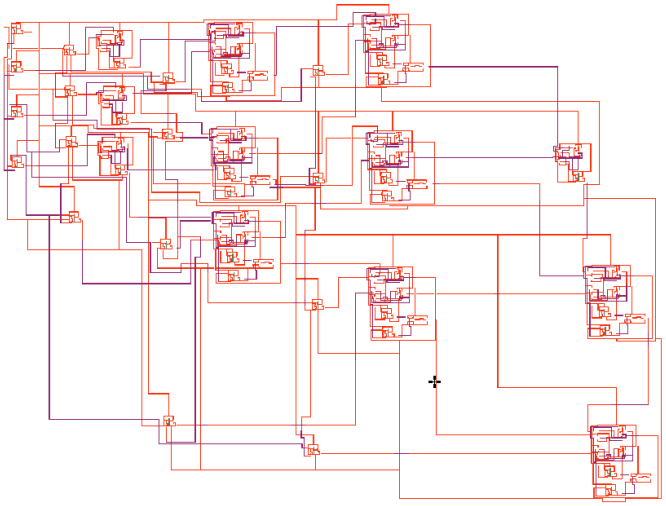

Fig 16: DPTL logic using array multiplier layout

8. CONCLUSION

In this paper, the proposed array multiplier is using full adder is simulated using 130nm CMOS technology. Typically power and delay minimizations techniques are important factors in VLSI domain. The proposed full adder cell provides more efficient in terms of area, power and delay when compared with the existing full adder cell. The proposed array multiplier performance increases compared with the existing array multiplier using full adder cell in terms of area, power and delay. In 130nm MOSFET technology, the proposed design uses less transistor count and saves 4.82% of total power, 120 w power dissipation, and exhibits more speed and less power delay product.

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