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On realization of a simple programmable frequency divider

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Abstract- Frequency dividers are widely used in frequency synthesizers and other synchronous clock based systems. In this paper a very simple and low-cost frequency divider with division ratio of 2^n, using off-the-shelf components, is presented. The circuit has been tested using software simulation as well as hardware implementations.

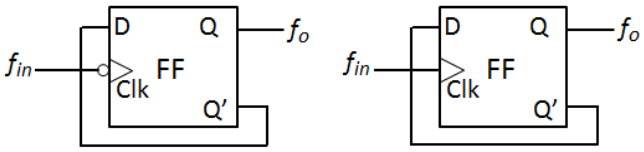
Key words: Counter, multiplexer, frequency divider.

I INTRODUCTION

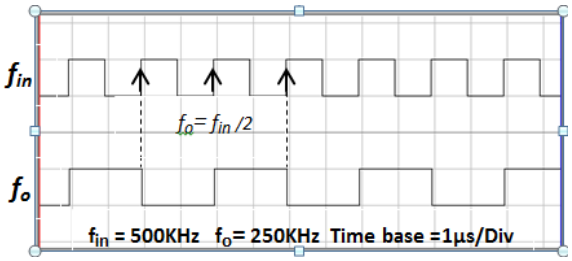
In Frequency hopping spread spectrum modulation based wireless communication systems, high resolution frequency synthesizers are widely used for generating different carrier frequencies [1]. In a Phase Locked Loop (PLL) based frequency synthesizer, the frequency multiplication is achieved through frequency division [2]. High resolution and wide range programmability are mainly determined by frequency divider. This demands a lot of circuit complexity and thus increases the cost of the system. Owing to the demand of better parameters, researchers and engineers have proposed many circuits in literature [3-5]. On the other hand, there are many other simple applications such as stepper motor based systems, electronic piano etc., where wide range programmability and high resolution of frequency dividers are not the main considerations but the low cost circuits are desirable. A simple circuit is proposed in this paper for such applications. The paper is organised as follows: In section II, a simple frequency divider circuit is discussed. Section III discusses the proposed programmable frequency divider. Finally, in Sections IV and V, results and conclusion are presented respectivey.

II FREQUENCY DIVIDER

The basic element for a divider circuit is shown in Fig.1 (a). Depending upon the nature of the flip-flop (FF), the output state can be forced to change from one state to another only either by rising edge or by trailing edge (but not both)of the clock signal. This property makes it to be used as a frequency division. As shown the input frequency is applied as a clock to the FF and at its output the frequency is divided by two as shown in Fig 1(b). As seen from the waveform, the output (Q) of the flip-flop changes from one state (say high to low) to another state (say low to high)only when the input frequency applied makes a transition from low-to-high.



(a)Trailing edgetriggered(b)Rising edge triggered



(c) Waveform

Fig 1: Basic frequency divider

A cascaded divided-by-2 frequency divider, known as counter, as shown in Fig. 2(a) provides various frequencies with the division ratio of N, where $N=2^n$, and n is the number of stages of flip-flops. A counter with n stages is shown in Fig. 2(b).

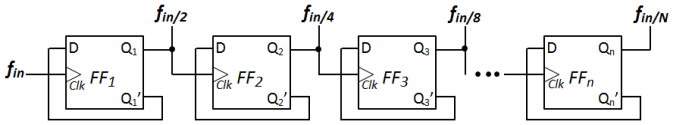


Fig 2(a) Rising edge triggered n-bit counter

For experimental investigation a 4-bit trailing edge triggered counter (IC7493) has been used. The outputs taken from the different stages are depicted from the waveforms shown in Fig.2 (d).As seen a division of $f_{in}/2^n$, i.e. 2, 4, 8, 16, can only be achieved. In order to obtain a division of f_{in}/n (where n=1, 2, 3, 4…..), a

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swallow counter based divider is required [5].This adds complexity to the circuit.

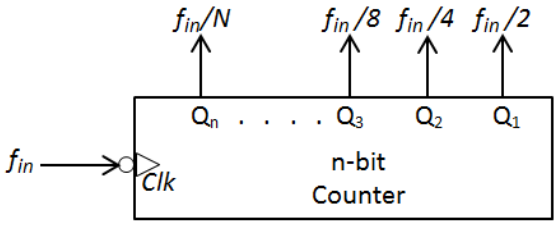


Fig 2(b): Trailing edge triggered n-bit counter

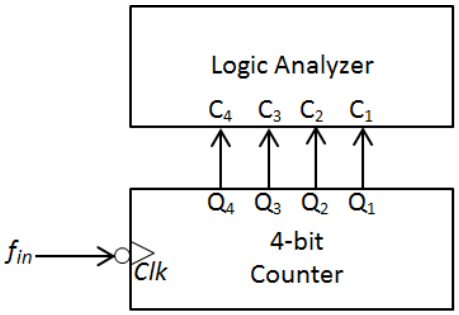


Fig 2(c): Trailing edge triggered 4-bit counter

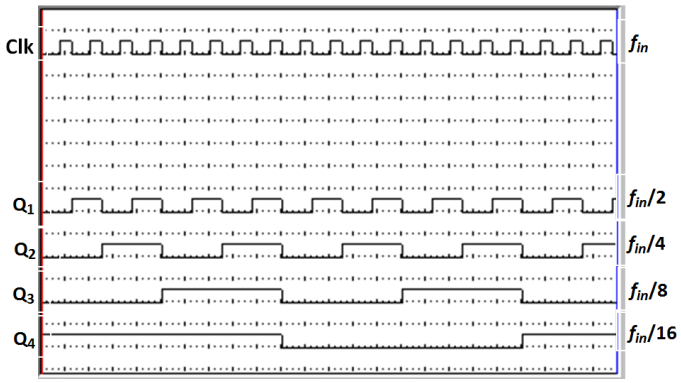


Fig 2(d): Waveforms obtained from counter

II PROPOSED CIRCUIT

The proposed circuit for programmable frequency divider is shown in Fig.3. It consists of a counter and a multiplexer. The outputs of counter are connected with the inputs of the multiplexer. As discussed in the previous section four different frequencies are available at the outputs of the counter.

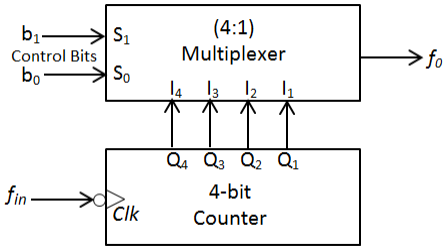


Fig 3: Proposed Circuit

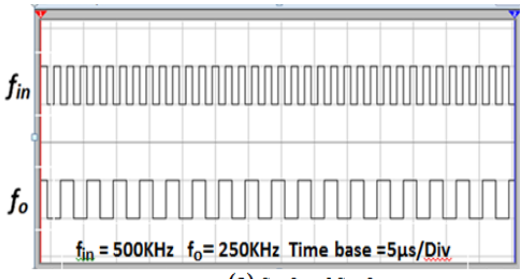
Any one of the frequency can be selected by applying a particular control word at the selection lines of the multiplexer. For example when s_1=0 and s_0=1, a divided by 4frequency can be achieved. Similarly other frequencies can be obtained by the application of different codes at selection lines as shown in table 1. Thus by programming the circuit any available frequency can be selected.

Table: 1

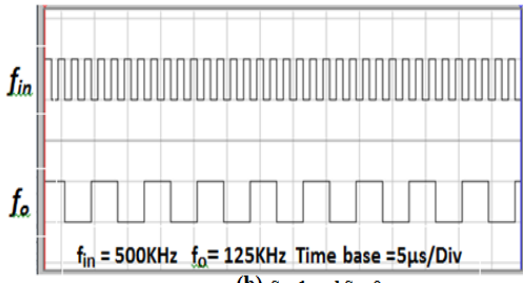
Control Word S_1	Control Word S_0	Counter Output	Output Frequency (f_o)
0	0	Q_1	$f_{in}/2$
0	1	Q_2	$f_{in}/4$
1	0	Q_3	$f_{in}/8$
1	1	Q_4	$f_{in}/16$

IIIEXPERIMENTAL RESULTS

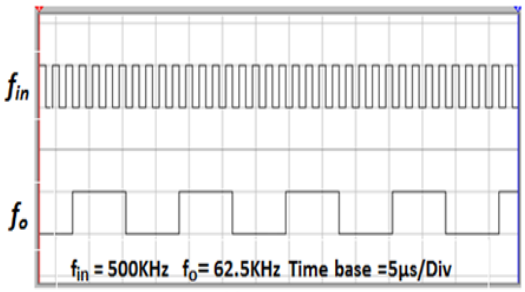
The workability of the proposed circuit was tested in simulations as well as in hardware implementation. IC 7493 was used as a counter and 74153 as multiplexer. The results obtained are shown in Fig.4. The reference frequency (f_{in}) of 500 KHz was obtained from a function generator.



(a) S_1=0 and S_0=0



(b) S_1=1 and S_0=0



(c) S_1=0 and S_0=1

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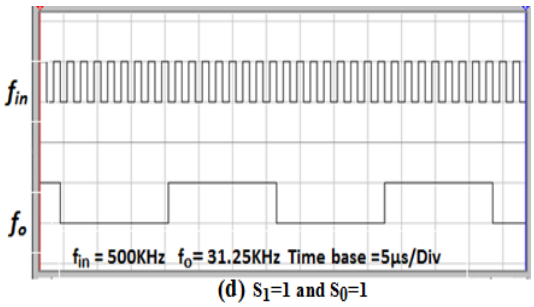

(d) S_1=1 and S_0=1

Fig 4: Waveforms of programmable divider

IV CONCLUSION

A simple circuit for frequency division is proposed in this paper. The circuit uses off the shelf components and can be used in the environments where a limited set of frequencies are required. The circuit can be used in undergraduate Laboratories for demonstration of various experiments.

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