ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 9, September 2017

Design of High speed CMOS current comparator

Ruthala. Kasi. Annapurna. Nageswari, Gollu. Vimalakumari

Abstract- The circuit design of high speed CMOS current comparator proposed in this paper. A new technique is discovered by Flipped voltage follower with voltage follower level shifter (LSFVF) is comparator input stage. The CMOS current comparator is design to reduce delay and improves the performance. The conventional current comparator is used for low power and low voltage applications. The comparators are compared in terms of parameters like delay, power dissipation and no. of transistors used. This circuit simulations were performed in CMOS 130nm Technology in MENTOR GRAPHICS TOOL.

Key words: current comparators, current mode circuits, flipped voltage follower, ADC's

1. INTRODUCTION

The current comparator [1] plays an important role in analog circuit design for current mode circuits, which is used to compare the two current signals. A fundamental component of current comparator used analog systems, i.e analog to digital converters (ADC'S), frequency converters etc. The comparators have particularly used in signal processing applications and data converters. The current comparator is need for reduce power consumption and increase the speed in VLSI circuits [3]. The current comparator proposed by`[4] traff's circuit shown in Fig.1(a),voltage follower used as comparator input stage i.e M1 and M2 transistors and M3 and M4 transistors used CMOS inverting stage amplifiers. The difference of two input currents I_{in} and V_{out} represents compared result between input current to output voltage. The input stage M1 and M2 transistors are turned off at this time increasing the input resistance, whenever the input current is high, and the current comparator dynamic response time increased.

Fig.1(b) the M5 and M6 transistors used to reduce the dead band region by using level shifters and the response time also reduced . However this current comparator circuit adding two biasing current sources, so the power consumption increased. A continuous time current comparator is used for low power applications and shorter delay time. The current comparator proposed by [7] MR transistor added to the resistive feedback network to the NMOS transistor. The proposed current comparator [8] one drawback the number of transistors increased and also increases more power dissipation.

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 9, September 2017

II. PROPOSED CURRENT COMPARATOR

a). COMPARATOR DESIGN

The schematic diagram of proposed current comparator circuit shown in Fig.1. This circuit consists of CMOS inverter, FVF with voltage follower level shifter (LSFVF) and input current, power supply. Here FVF with VF level shifter is used to reduce the delay.

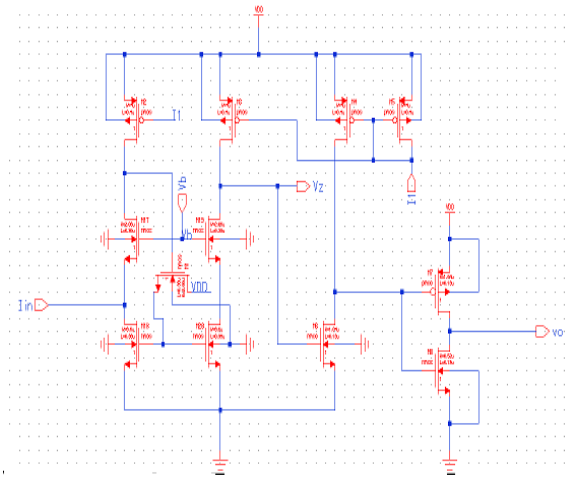

Fig. 1 Proposed CMOS current comparator

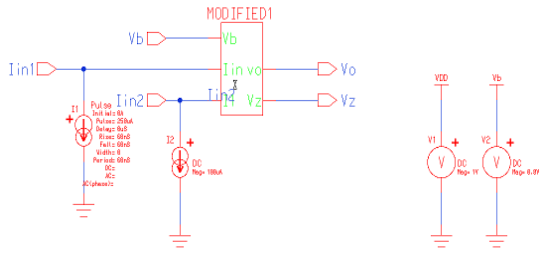

Fig. 2 Simulation of proposed current comparator

b). FVF with VF level shifter (LSFVF)

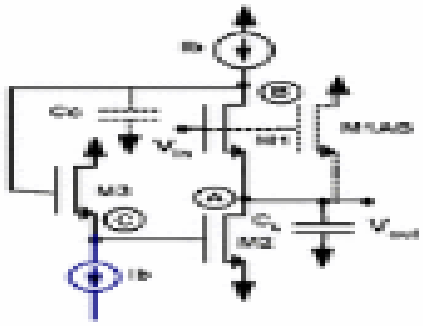

Fig. 3 FVF with vf level shifter

The voltage follower is one of the basic building block of analog circuits, a gate source voltage of M1 transistor biased on the source side, with a constant current source I_b.

The key element FVF is replace by FVF with voltage follower level shifter (LSFVF) is used, the level shifter include transistors M1 and M2 is drain and gate terminals. The proposed current comparator is used FVF with voltage follower level shifter (LSFVF) is large output voltage compared to the conventional current comparator.

$$I_{ref} = \frac{\text{current input range}}{2^{n}-1}$$

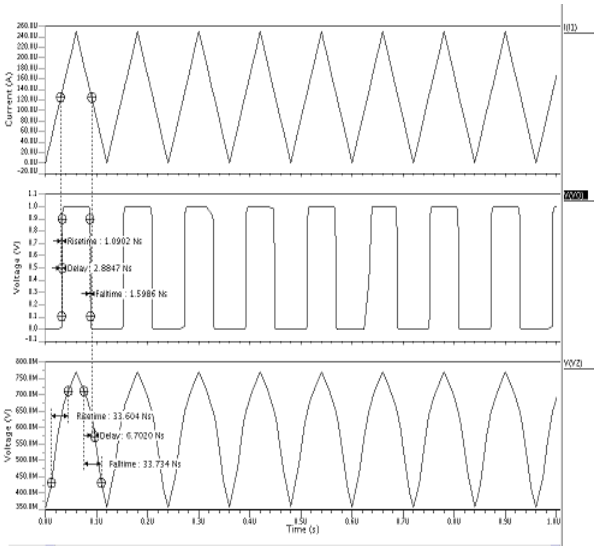

Fig.4 Proposed comparator simulation results

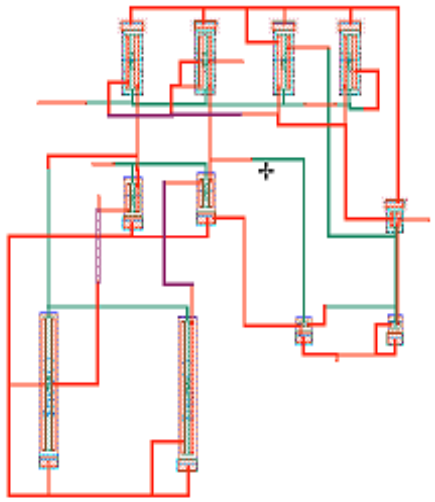

Fig.5 Proposed current comparator layout in 130 nm technology

The current comparator implementation flipped voltage follower with an NMOS inputs differencing two currents i.e input current I_{in} and reference current I_{ref}, one output voltage V_o.

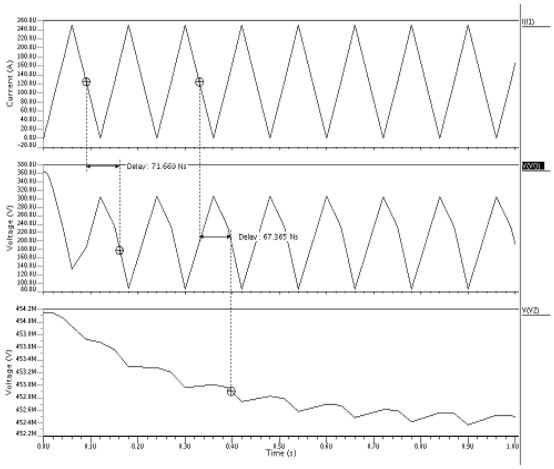

Fig.6 Post layout simulation of proposed current comparator

Table.1: Comparison between different current comparators pre-layout simulation

parameter	Conventional current comparator 1	Conventional current comparator 2	Proposed current comparator
Delay	74.951 ns	4.383 ns	2.88 ns
Power dissipation	119.025 u watts	145.19 u watts	245.25 u watts
No. of transistors	10	11	12

Table.2: Comparison between different current comparators post-layout simulation

Parameter	Conventional current comparator 1	Conventional current comparator2	Proposed current comparator
Delay	76.45 ns	64.2 ns	42.46 ns
Power dissipation	119.025 u watts	145.19 u watts	334.25 u watts
No. of transistors	10	11	12

III. CURRENT MODE FLASH ADC

An application of a 3- bit current mode flash ADC is implemented as shown in Fig.7. Where input current represents I_{in} and reference current represents I_{ref} .The current comparator to be employed for 3-bit conversion is given by 7 inputs. The current comparators consist of two currents, one

is input current and another one is reference current. Each comparator input current I_{in} compares with its successive reference current I_{ref} , hence all the current comparators comparison in parallel, so this structure is also called as a parallel analog to digital converter (ADC). The comparator output converted into thermometer code to corresponding binary code by a7×3 encoder blocks. The comparator inputs are C7 (MSB) to C1 (LSB), the encoder outputs are B2 (MSB) to B0 (LSB), respectively.

The 7×3 CMOS encoder, shown in below Fig.8, has been designed for thermometer to binary conversion which remains the same for these entire current mode flash ADC's.

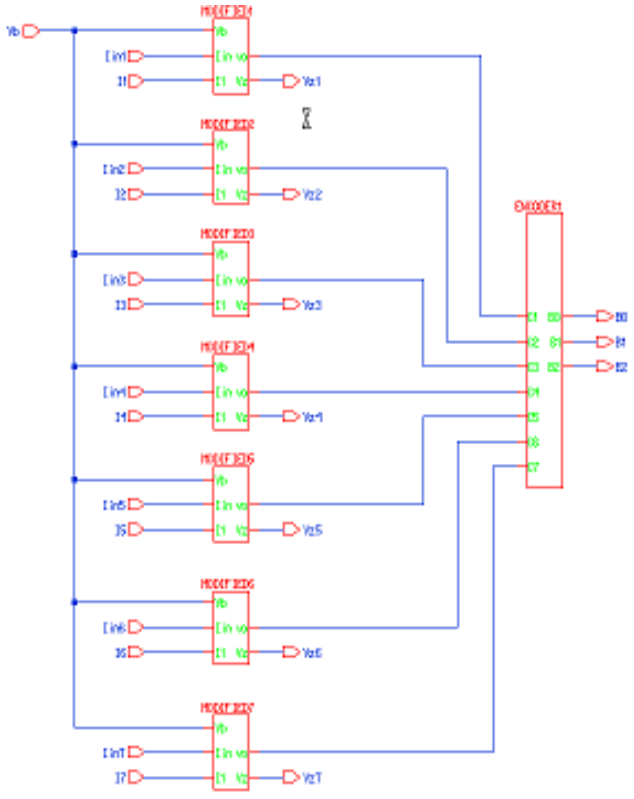

Fig.7 3-Bit Current mode Flash ADC

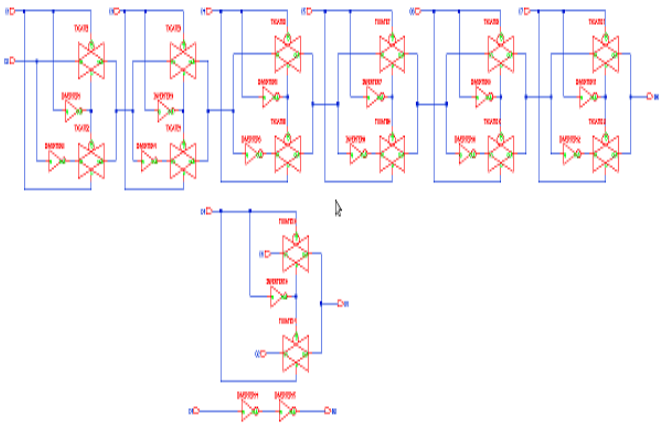

Fig.8 7×3 CMOS encoder

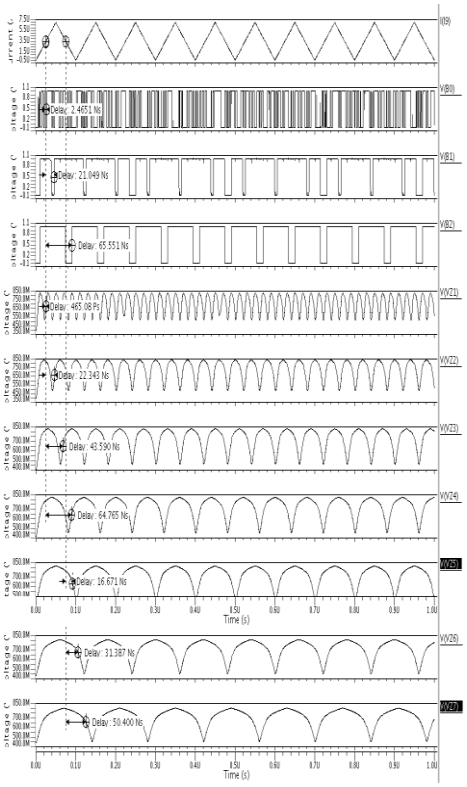

Fig.9 Pre layout simulation results of CM Flash ADC

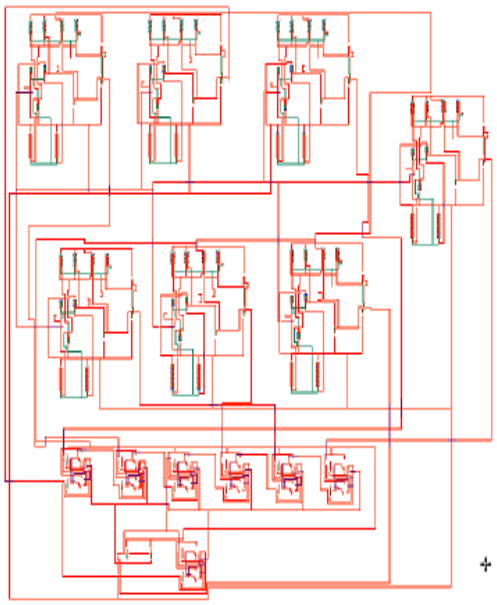

Fig.10 Layout of 3-bit current mode Flash ADC

Table.3 3- bit current mode flash by using FVF technique for pre-layout simulation

parameter	Conventional current comparator 2	Proposed current comparator
Delay	481.87 ps	458.34 ps
Power dissipation	688.3901 u watts	541.725 u watts

Table.4 3- bit current mode flash ADC by using FVF with VF level shifter technique for post – layout simulation

parameter	Conventional current comparator 2	Proposed current comparator
Delay	1.2301 ns	944.04 ps
Power dissipation	782.595 u watts	548.72 u watts

IV. SIMULATION RESULTS

The FVF with VF level shifter is used to the proposed current comparator circuit is simulated using 130nm CMOS technology. Here 1V (Vdd) supply voltage is taken for both pre layout and post layout simulation. The FVF with VF level shifter circuit offers less propagation delay, and also this circuit provides 2.88ns delay and 245.25uw power dissipation at input current pulse of 250uA.

V. CONCLUSION

High speed CMOS current comparator presented in this paper. The delay is comparable to existing current comparator. Here the flipped voltage follower with voltage follower level shifter technique is used to the comparator input stage. The application of 3-bit current mode flash ADC is used high speed response and low power applications. The simple structure makes this circuit suitable to high speed response.

REFERENCES

[1]. Jesus Ezequiel Molinar Solis, Marco Gurrola Navarro, Israel Mejia"Low Input Resistance CMOS Current Comparator Based on the FVF for Low-Power Applications" , IEEE ckts and systems, vol. 39, no. 2, spring 2016.

[2]. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques," IEEE Circuits Syst. Mag., vol. 2, no. 1, pp. 24–42, 2002.

[3]. Traff, "Novel approach to high speed CMOS current comparators," Electron. Lett., vol. 28, no. 3, pp. 310–312, Jan. 1992.

[4]. A.T. K. Tang and C. Toumazou, "High performance CMOS current comparator," Electron. Lett., vol. 30, no. 1, pp. 5–6, Jan. 1994.

[5]. X. Tang and K.-P.Pun, "High-performance CMOS current comparator," Electron.Lett., vol. 45, no. 20, pp.1007–1009, Sep. 2009.

[6]. B.-M. Min and S.-W.Kim, "High performance CMOS current comparator using resistive feedback network," Electron.Lett., vol. 34, no. 22, pp. 2074–2076, Oct. 1998.

[7]. R.G. Carvajal et al., "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 7, pp. 1276–1291, Jul. 2005.

[8]. L. Chen, B. Shi, and C. Lu, "Circuit design of a high speed and low power CMOS continuous-time current comparator," Analog Integr. Circuits Signal Process., vol. 18, no. 3, pp. 293–297, 2001.

[9]. AJaime Ramirez-Angulo,MariaRodamas Valero- bernal Antonio lopez-martin" class AB output stages for low voltage CMOS op amps accurate quesient dynamic baising IEEE Transactions and systems 152,1276-1291(2000).

R.K.A Nageswari she has received her B.E Degree in Electronics and Communication form A.S.K College of Engineering, Visakhapatnam, Andhra Pradesh, India in 2014. She is presently pursuing M.Tech 2nd Year in M.V.G.R College of Engineering (A) located at Vizianagaram which will be completed in 2017. Her research interests including Analog and Digital Communication.

Mrs. G.Vimala Kumari Pursuing Ph.D in JNTU Kakinada. She is working as Assistant Professor in Department of Electronics and Communication Engineering, M.V.G.R College of Engineering Vizianagaram, Andhra Pradesh, India. She has 10 years of Teaching Experience in Engineering college. Her research interests include VLSI image processing and Communication Systems. She is member in various professional societies such as IE.