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Fabrication of Si based memory using 6x6 array of memristers

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***Absract*:**
This paper describes the fabrication of memory device using 6x6 array of memristor devices based on titanium. A memristor is a two-terminal device with a variable resistance that can be used as memory. This memristor is implemented on silicon substrate by sandwiching Titanium Oxide, a thin layer (in nanometer) between two plates of Ti gold which act as electrodes. The Titanium Dioxide acts as the resistive material. Characterization and fabrication with the lowest possible dimension of the memristor is carried out. Also achieving low power dissipation and implementing with modern tools and processes in nano electronics was the main motto of our achieved target.

Keywords— Memristor, TiO_2, electron beam lithography, memory, fabrication

I. Introduction

In VLSI (Very large scale Integration) design Moore's law is followed successfully. There are physical and economical limitations in CMOS scaling. The dimensions of devices are required to minimize at same time the devices should be efficient. There is a need of innovative fabrication technologies, advanced material research.

A memristor is a two-terminal device with a variable resistance that can be used as memory. A memristor changes its resistance between two values and this achieved via the movement of mobile ionic charge within an oxide layer [1].At first it was thought that memristors could not perform a full set of logic operations but it has now been found that a memristor can utilize other memristors to reprogram themselves in a manner that memristor circuits could be used, not just for memory retention, but as CPUs as well. Memristors are the devices utilize high and low resistance states. This device exhibits current-voltage hysteresis that depend on the magnitude, polarity, and time duration of the applied voltages.

Titanium dioxide (TiO_2) has a wide energy band gap of 3.2eV so that its absorption normally occurs by the ultraviolet light. TiO_2 have been broadly used because of its high stability, low cost, relatively low toxicity and excellent photo catalytic performance in comparison to other semiconductor materials. The memristor is implemented on silicon substrate by sandwiching Titanium Oxide, a thin layer (in nanometer) between two plates of Platinum which will acts as an electrode. The Titanium Dioxide will acts as the resistive material. Characterization and fabrication with the lowest possible dimension (width/length (w/l) ratio of oxide layer) of the memristor is the main task.

Memristor technology also promises dense, compact memory packages, on par with the density capability of a biological brain. Already HP labs have designed circuits that mimic aspects of the brain. Transistors are used as neurons, nano wires in a crossbar network act as axons and the memristors at the cross points act as synapses. In the future, even the transistors might be replaced by memristors. Memristors can be made extremely small, at nanometer scales.

Recently, device scaling has slowed down, while electrical interconnect has become both a performance bottleneck and a major source of power dissipation, which is currently the most critical limiter for technology growth. Conventional memory technologies, such as Flash, DRAM, and SRAM, are unable to keep up with market requirements for higher density and lower power. Flash memory has already achieved its physical limits, and cannot be scaled further, primarily due to its limited endurance.

These problems can be addressed by emerging new semiconductor devices, such as memristors, which are useful both as memory cells and as novel switching circuits. Hence proposed memory cell with as low as possible dimension, low power dissipation and implementation with modern tools and processes is the main motto of our project.

II. Experiments

The current knowledge-based society requires a new, more- powerful memory technology for the development of any field concerning human activity, such as biomedicine, space research, meteorological predictions, simulation in basic research science, and entertainment. Nowadays computers use two types of memory, i.e., dynamic random-access memory (DRAM) and static random-access memory (SRAM). The handicap of these fast memories is that they are volatile, i.e., data are lost when the power supply is removed. For this reason computers also use a nonvolatile memory, i.e., hard-disk drives (HDDs). HDDs are nonvolatile but also slow, thus increasing the computer start-up time. Another kind of nonvolatile memory commonly employed for data storage in hard disks, digital cameras, USB memory sticks, or cellular disks is Flash memory. Its main drawbacks are a slow writing speed and the limited number of write/erase cycles that can be endured. This paper describe fabrication of non-volatile memory using memristor arranged in 6x6 array as shown in Fig 1.

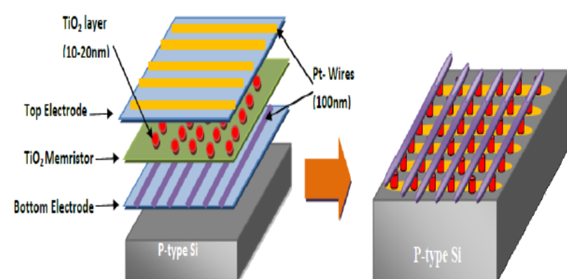

Fig.1: 6x6 memory using 6x6 array of memristor devices.

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III. Fabrication

Fabrication of this memory is done using nano fabrication technology processes in Nano Lab center at IIT Bombay. The nanofabrication steps include Pattern generation, electron beam lithography, sputtering, etching/liftoff and metallization. Fallowing Fig. 2 shows process flow for memory design.

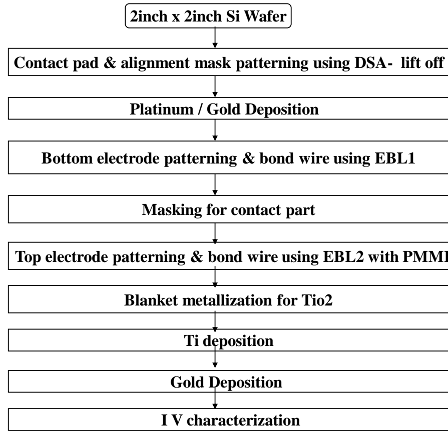

Fig. 2 Process flow for memristor design

Device dimension depends on thickness of TiO_2 which was approximated from 10nm to 22nm initially.In this memory thickness of $TiO_2$is 10nm.Thickness of platinum/ gold is set to50 nm.

Figure 3 shows the cross sectional layout of memristor. On silicon wafer, Tio_2 of 10 nm thick is sandwiched between two platinum/ gold layer of 50nm with 20nm thick Ti acts as an electrode1 and Electrode2 respectively.

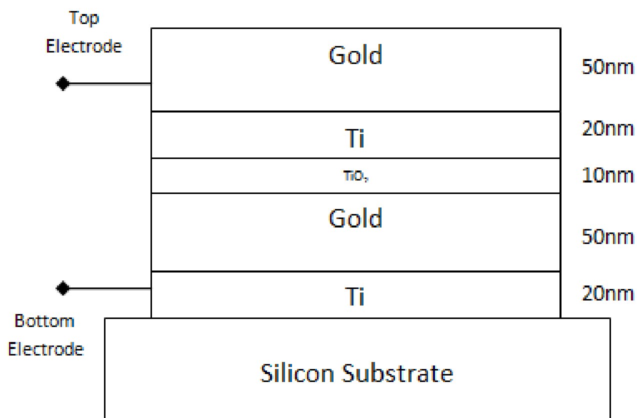

Fig. 3 cross sectional layout of memristor

On Si wafer electron beam lithography (EBL) is carried out to obtain the pattern for Ti gold i.e. EBL1.For this raith 150 two unit is used with4 target e-beam evaporator. This focuses on the physics underlying the e-beam lithography process and our e-beam lithography tool - Raith 150 Two. It begins with the fundamental reasons for moving towards e-beam lithography and moves onto how an e-beam lithography tool essentially works. It details some of the important concepts of tool working such as beam spot size and astigmatism. Further, performance specifications and test results obtained using the Raith 150 Two tool have been outlined. A mask is used to cover the contact pads and EBL 2 with PMMA is carried out.Before EBL2 sample was placed on PMMA spinner with 3000rpm speed.For thisPMMA with 950K ,4% wasused.Fig.4 shows images of our target after EBL1 AND EBL2. It has been done with 4 target e-beam evaporator because of lift off issues.

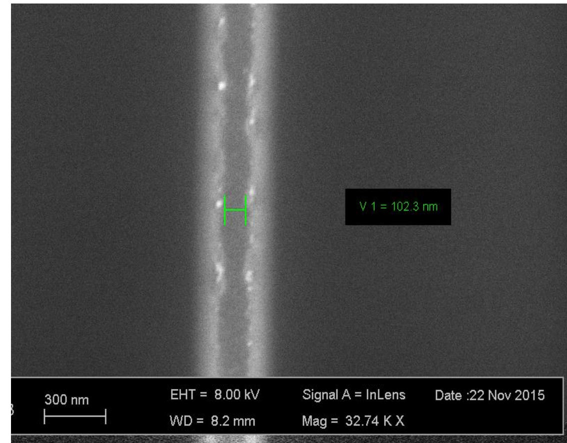

Fig. 4.a

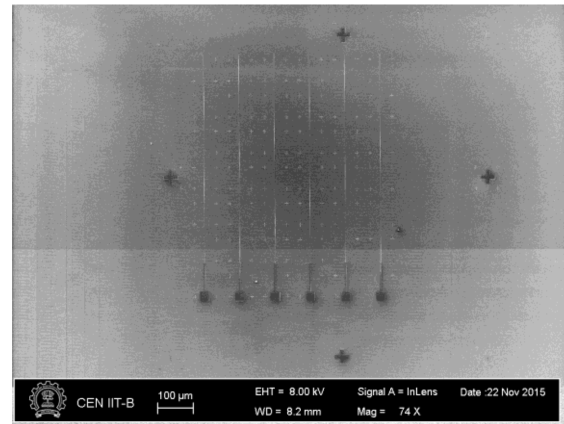

Fig. 4. b

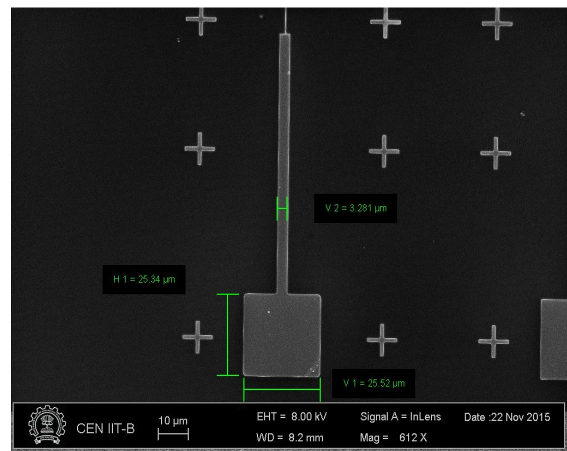

Fig. 4.c

Fig. 4.: a) nanowire array of 100nm. b)Image after EBL1. c) Contact pad image

Then blanket metallization is done for TiO_2. 10 nm TiO_2 is deposited with orion sputter at 15nm/minute of deposition rate. . The TiO_2 film is deposited using AJA Orion Sputter

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System at 400°C. Then Ti of 20nm and then Gold of 50nm is deposited to form the memristor structure. MJB4 e-beam lithography is used to cover contact pads. The MJB4 Mask Aligner can perform contact UV exposures for a variety of sample and mask sizes. Sample sizes that can be accommodated range from small pieces to 4 inch wafers. It can be used with masks of up to 5 by 5 inches. The maximum combined thickness of the substrate and mask is 9 mm. The achievable position alignment accuracy is ~1 µm. The MJB4 allows 1 um resolution in vacuum contact mode. The tool had 5 different contact modes (proximity, soft, hard,low vacuum, and vacuum), and three different exposure modes (flood, first, and align and expose).

A 6x6 matrixarray is designed for memristor. Total 36 devices are fabricated on the wafer within 1000µm x 600µm as shown in Figure 5.

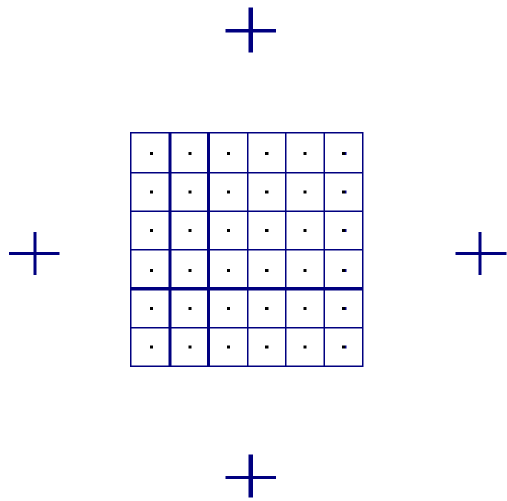

Fig. 5: A Memory with 6x6 matrix array for memristor.

Figure 6 shows the designed memory with 6x6 memristor array.

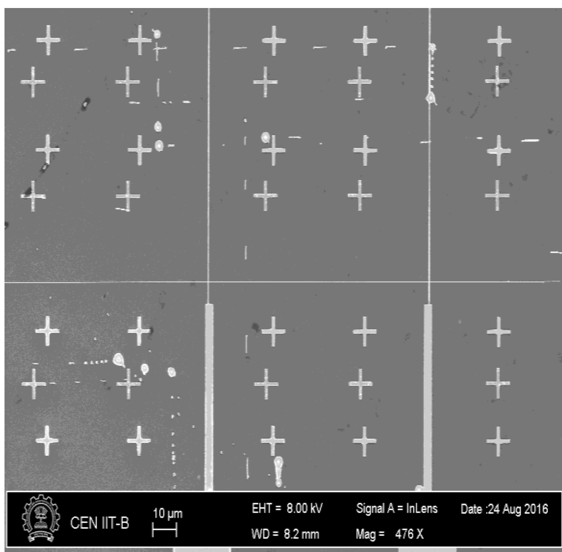

Fig. 6: memristor array (Raith 150)

The complete target is cleaned with acetone and then drieda and carried out for characterization.

IV. Results and Discussion

The designed memory with memristers array then brought to PROXIMA PM8-SUSS Microtech unit.

The typical *I-V* characteristics of the memristor device is displayed in Figure7. When the voltage ischanged back and forth (-2V-0V- +2V), it is seen that the deviceexhibits the Hysterisis. Experimented Voltage dependent switching characteristics is found similar to characteristics of memristors.

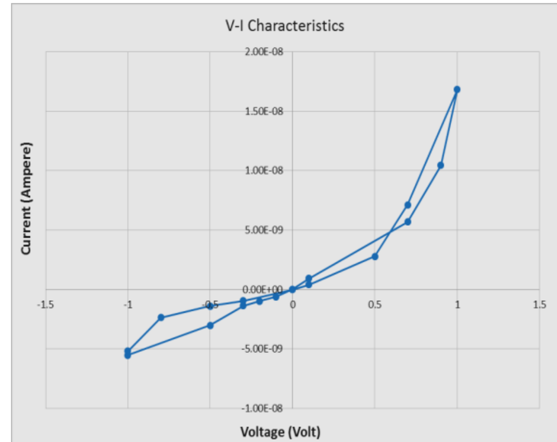

Fig7: I-V Characteristics of memristor

Following table 1 shows resistance and power dissipation for current exerted by memrister device depending on voltage applied.

Table 1 : Resistance and Power dissipation for current exerted by memrister device depending on voltage applied.

Sr. No.	Voltage (Voltage)	Current (Ampere)		Power
				5.170 nW

V. Conclusion

This paper describes memory designed with metal oxide based memristor, its fabrication, and characterization. .With successful implementation of memory device, TiO_2 proved its high stability, low cost, relatively low toxicity and excellent photo catalytic performance in comparison to other semiconductor materials. The memristor designs are based on oxygen deficient titanium oxide stacked with another metal oxide such as chemically stable titanium oxide. From the results for each memristor design, the titanium oxide device exhibits bipolar characteristics of memristive performance. The behavior of TiO2based memristor array is demon strated. By controlling different positive and negative voltages, the memory device has the potential ofstorage because of

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hysteresis experimented..As voltage increases from 0 to 1 volt, current increases and resistance decreases.For 1 volt current exerted is 16.8nanoAmpere with 59.52 Mega Ohm of resistance.During negative sweep as voltge increases, current decreases and resistance increases. For -1 volt current is -5.17 nano Ampere with 1934.2Mega Ohm of resistance. Behavior of memory device is found to be linear in both, positive and negative sweep. The best hysteresis is exerted for -1volt to 1 volt. This is the pinched hysteresis loop(-1volt to 1 volt) and is considered as a fingerprint of the memristor.

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