ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 11, November 2017

Performance Analysis of Current Starved VCO in CMOS 45 nm process Technology using Cadence Tool

N SANDEEP[1], P SRAMIKA REDDY[2]

Abstract: **This proposed paper focuses on design and analysis of Current Starved Voltage Controlled Oscillators (CSVCO) using 45nm CMOS technology. Voltage Controlled Oscillators can be built using a vast number of circuit techniques. The design and implementation of the proposed is performed using Cadence CAD (Computer Aided Design) tool in 45nm process technology. VLSI CMOS circuits work on low power during static application and the same functionality can be implemented with a bit denser circuits. The reference frequency is 50 MHz with 0.9 V input control voltage. In Current Starved voltage controlled oscillators, the voltage controls the output frequency of the oscillator. The Simulation results and performance analysis for Current Starved Voltage Controlled Oscillator is done in this paper.**

Index Terms: CMOS, VCO, Cadence Tool, CSVCO

I. INTRODUCTION

VCOs using CMOS process technology is used for low frequency applications whereas submicron processes have allowed CMOS oscillators to achieve frequencies in the GHz range[1]. A VCO is the heart of the PLL and can be designed either by LC or RC. An LC type has superior phase noise performance compared with ring VCO whereas an LC type has a small tuning range large layout area and possibly higher power for applications including clock and data recovery, microprocessor clock generation and frequency synthesizer, Phase-locked loops are used that generate well-timed on-chip clocks[5] . The ring oscillators do not have the complication of the on-chip inductors required for the LC oscillators and hence the chip area is reduced..

II. CURRENT STARVED VCO

This current starved VCO is designed using ring oscillator. A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. The ring oscillators do not have the complication of the on-chip inductors required for the LC oscillators and hence the chip area is reduced [3]. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. From the schematic in Figure 1, it is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for the current[6].

The MOSFETs M5 and M6 drain currents are the same and are set by input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. [2].

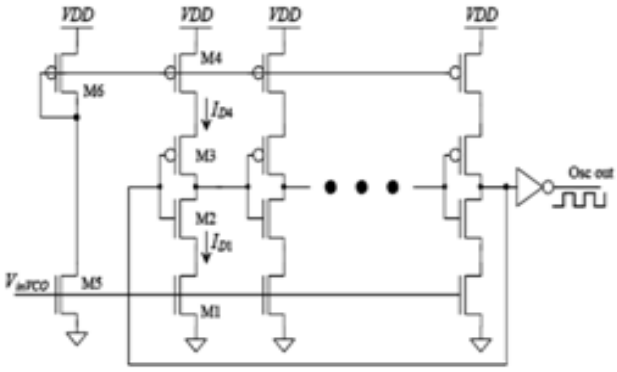


Figure 1: Current Starved VCO [2]

III. CALCULATIONS

The average power dissipated by the VCO is

$$P_{avg} = V_{DD}.I_{avg}$$

If we include the Power dissipated by the mirror MOSFET M5 and M6 the power is doubled from the average power dissipated equation, assuming that $I_D = I_{D5} = I_{D6}$

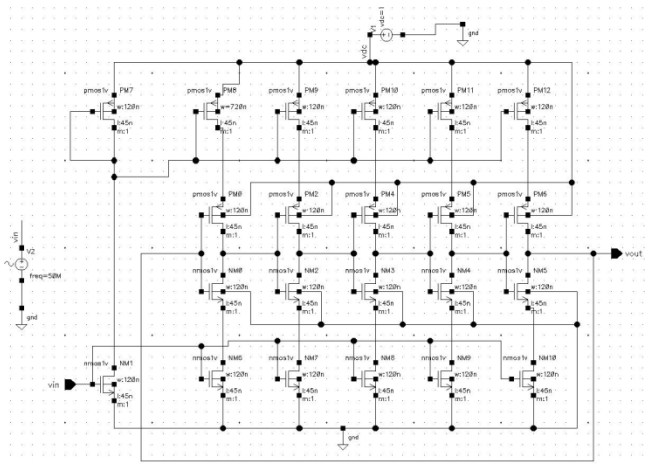
For low power dissipation we must keep I_D low which is equivalent to stating that for low power dissipation we must use a low oscillation frequency[2]. The practical value of the input resistance of the VCO is infinity, whereas the input capacitance value is very small compared to the loop filter capacitance values.

Manuscript received Nov, 2017.

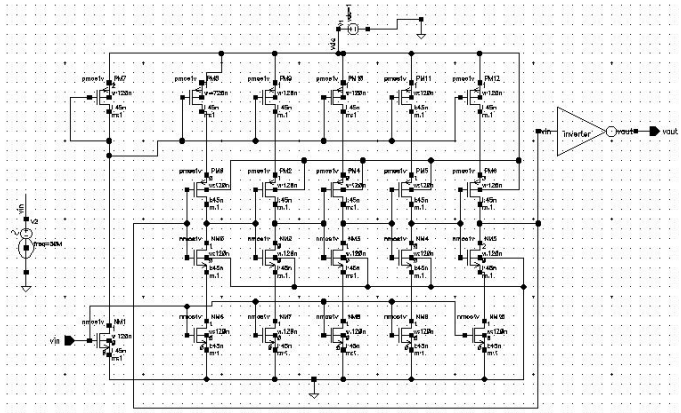
N SANDEEP*, Assistant Professor, Electronics and Communication Engineering, SreeNidhi Institute of Science & Technology, Hyderabad, Telangana, India.*

P SRAMIKA REDDY*, Assistant Professor, Electronics and Communication Engineering, SreeNidhi Institute of Science & Technology, Hyderabad, Telangana, India*

ISSN: 2278 – 909X
International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)
Volume 6, Issue 11, November 2017



(a)



(b)

Figure 2: Schematic of current starved VCO

PMOS transistors: PM0, PM1, PM2, PM4, PM5, PM6, PM7, PM8, PM9, PM10, PM11, PM12.

NMOS transistors: NM0, NM1, NM2, NM3, NM4, NM5, NM6, NM7, NM8, NM9, NM10, NM11. (one pair of these forms an inverter).

The circuit consists of 22 transistors that constitute a 5 stage voltage controlled oscillator capable of generating a signal with output frequency in the range of 3GHz to 6 G Hz.

The oscillation frequency of current starved VCO for number of stages(N) greater or equal to five can be given by

$$f_{osc} = 1/N(t_1+t_2) = I_D/(N.C_{tot}.VDD)$$

The oscillations of the VCO stops when the input voltage of the VCO is less than the threshold voltage of the transistors[4].

$$V_{min} = V_{THN} \text{ and } f_{min} = 0$$

IV. SIMULATION RESULTS

The output waveforms obtained from the transient response analyzed between the output voltage and input control voltage vs. time in ns.The frequency of the output signal is observed to be in the range of 3GHz to 6 GHz depending upon the variations in the input control voltage. The waveform in the figure 3 is obtained with a frequency of 3.405GHz for an input control voltage of 0.9V and supply voltage of 1V and the output power is observed to be 0.255E-6W with output current of 0.215E-6A.

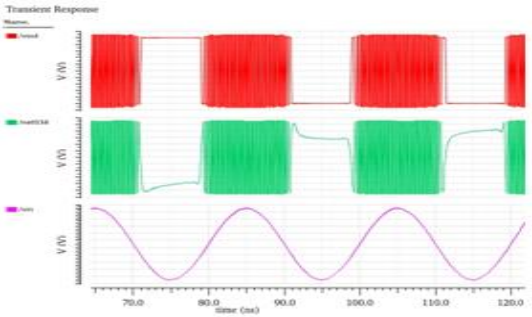


Figure 3: Transient response of VCO

The waveform in the figure 4 is obtained with a frequency of 5.620GHz for an input control voltage of 0.9V and supply voltage of 1.3V and the output power is observed to be 0.5569E-6W with output current of 0.5988E-6A.

The waveforms shown in figure 5 are observed during analysis of CSVCO. The observations include the variations in the output frequency signal generated with respect to 2 the variations in the input control voltage applied to the CSVCO.

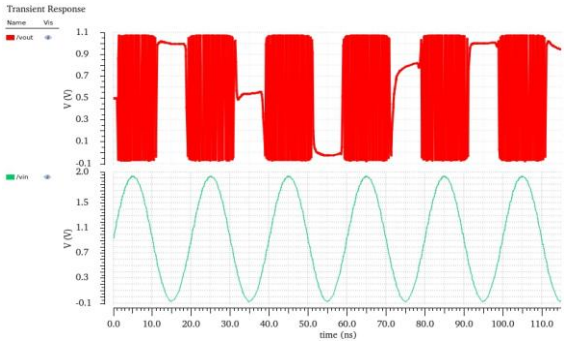
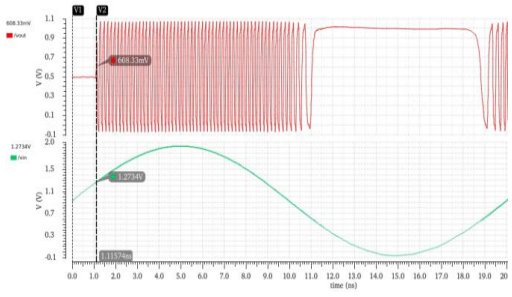
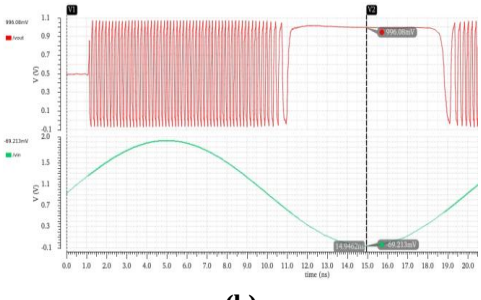


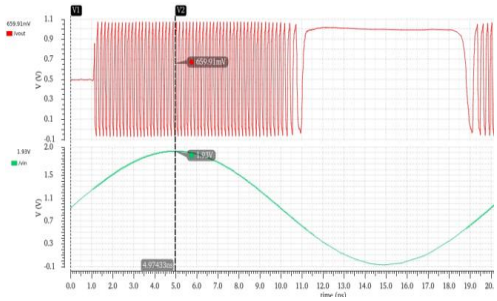
Figure 4: transient response of VSVCO



(a)



(b)



(c)

Figure 5: waveform showing output frequency variations with respect to input signals at various instants

Control Voltage (V)	input freq (MHz)	output freq (GHz)	output power (uW)	output current (uA)
0.95	50	5.621	0.5569	0.6683
0.94	50	5.198	0.429	0.5148
0.93	50	4.829	0.369	0.4428
0.92	50	4.212	0.3211	0.3853
0.91	50	3.967	0.269	0.3228
0.9	50	3.405	0.2554	0.3065

Table1: Variations observed in output parameters due to changes in input control voltage

V. CONCLUSION

The analysis of Current Starved Voltage Controlled Oscillator (CSVCO) using 45nm CMOS technology has been proposed in this paper using CADENCE Virtuoso schematic editor and spectrum analyzer. The main focus of this paper is on power consumption and output frequency. CSVCO consume less power in the range of 255nW along with output frequency in the range of 3GHz to 6 G Hz.. The simulation results obtained shows reasonably good frequency stability.

REFERENCES

[1] M. Banu, "MOS oscillators with multi-decade tuning range and gigahertz maximum speed", IEEE Journal of Solid-State Circuits, vol. 23, pp. 1386–1393, December 1988.

[2] R. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout and Simulation," IEEE Press Series on Microelectronics Systems, pp. 355-361 and383-387, 2000.

[3] B. Razavi, "Monolithic phase-locked loops and clock recovery circuits-theory and design", IEEE Press,pp. 283-377 and 381-483, 1996

[4] M. Jamal Deen, "Ultra Low-Voltage Low-Power Voltage Controlled Oscillator", Electrical and Computer Engineering Department, CRL 226 McMaster University, Hamilton, ON, Canada L8S 4K1.

[5] M. J. Underhill, "Fundamentals of oscillator performance", Electronics and Communication Engineering Journal, vol. 4, no. 4, pp. 185-193,

[6] "A Large Tuning Range Ring VCO in 180nm CMOS"
Xuemei Lei, Progress In Electromagnetics Research Symposium Proceedings, Taipei, March 25 - 28, 2013

[7]B. P. Panda, p. K. Rout, d. P. Acharya and g. Panda "Design of a novel current starved VCO via constrained geometric programming" april 12- 14 2011 international symposium on devices mems intelligent systems communications 2011.

***N SANDEEP**, Assistant Professor,*
M.Tech VLSI and Embedded Systems
Gold Medalist,
Electronics and Communication Engineering,
SreeNidhi Institute of Science & Technology,
Hyderabad,
Telangana, India

***P SRAMIKA REDDY**, Assistant Professor,*
M.Tech VLSI and Embedded Systems
Electronics and Communication Engineering,
SreeNidhi Institute of Science & Technology,
Hyderabad,
Telangana, India