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VLSI Technology used in Auto-Scan Delay Testing Design For Bench Mark Circuits

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ABSTRACT:— Auto scan, a design for testability (DFT) technique for synchronous sequential circuits. Scan operation under auto scan improves circuit testability by allowing the shift operations. In this work, without external scan inputs or outputs are presented that aims to achieve maximum fault coverage's and to reduce the test application time in circuits. Auto scan uses random test sequences, because random test patterns covers more fault coverage's than sequential test patterns. Linear feedback shift register (LFSR) is widely used for generating the random test patterns. Experimental results for various bench mark circuits are given to show the effectiveness of this method. The proposed method is to find the delay faults that occur in a given circuit and hence, the results can be simulated by using Xilinx 12.1.

KEY WORDSDesign for testability (DFT), Linear feedback shift register (LFSR)

1. INTRODUCTION

Since the electronics technology accomplished higher levels of integration into a single Silicon chip that led to Large Scale Integration (LSI), which preceded VLSI, the applications of electronic systems have experienced an almost unlimited expansion. However, despite the many advantages provided by VLSI, the inherent high integration level started to necessitate very sophisticated testing strategies in order to verify the correct device operation. As the electronics market stimulated the use of VLSI in a variety of tasks from critical military applications to consumer products, the reliability of the products functioning gained an escalating importance.

The expanding demand for ASIC applications led to development of more sophisticated Computer Aided Design (CAD) tools; which have shown most significant progress in layout and simulation, with yet more inferior improvement in testing. This consequently leads to designs with superior complexity, but which are in contrast extremely difficult to test effectively. Moreover, due to the low volume attribute of ASICs, the high test costs cannot be retaliated with large amounts of mass production.

A. FUNCTIONAL AND STRUCTURAL TESTING

Before structural testing was proposed, digital systems were tested to verify their compliance with their intended functionality, i.e. in this philosophy, a multiplier would be tested whether it would multiply and so forth. This testing philosophy is termed as functional testing, which can be defined as, applying a series of determined meaningful inputs to check for the correct output responses in terms of the device functionality. Although this methodology imparts a good notion of circuit functionality, under the presence of a definitive fault model, it is very difficult to isolate certain faults in the circuits in order to verify their detection.

B. DESIGN FOR TESTABILITY

We can significantly improve circuit testability by decomposing the design into smaller circuit modules that can be tested more easily. Circuit modules are easy to test when only a few test vectors are needed to be sure that the module is fault free. Generating tests for circuit modules is beyond the scope of this class. We instead will take the point of view that a circuit structure that gives easy access to the internal nodes of the circuit can usually be tested with only a few test vectors. Access to internal nodes is easy when you construct the circuit out of discrete components on a prototyping board. This is not physically possible inside

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an integrated circuit. We are restricted to using the signals on the bonding pads of the circuit.

C. AN ATPG FLOW TO GENERATE CROSSTALK-AWARE PATH DELAY PATTERN

An Automatic Test Pattern Generation (ATPG) flow to test path delay fault by simultaneously coupling multiple aggressors surrounding a delay sensitive victim path. This flow uses the most effective aggressors for pattern generation based on crosstalk information predetermined from the layout of the circuit. We developed the constrained ATPG flow by customizing the existing scan-based techniques to generate functionally testable path delay faults.

II. PROPOSED SYSTEM

The TIMED Flip-Flop provides the capability of error detection and correction by appending only a multiplexer (MUX-B) and a XOR gate in the structure of the standard (main) scan Flip-Flop.

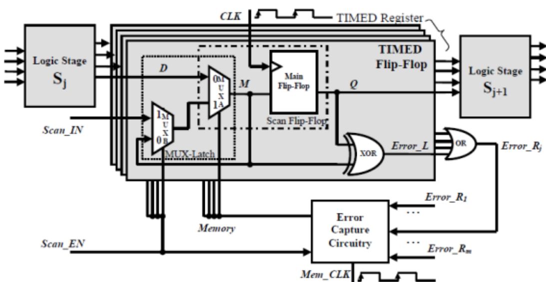

Fig. 1. Time Dilation Architecture

When the scan enable signal (*Scan_EN*) is “high” the TIMED Flip-Flop operates like a scan Flip-Flop to support the pertinent off-line testing activity. In the normal mode of operation (*Scan_EN*=“low”) the TIMED Flip-Flop behaves like an ordinary Flip-Flop enhanced with the ability to detect and correct timing errors. The XOR gate is used to directly compare the data at the *M* input and the *Q* output of the Main Flip-Flop for error detection, while the two multiplexers and the feedback path from the *M* line to the input of the additional MUX-B forms the required memory element (MUX-latch) that holds valid data for error correction.

Briefly, the Time Dilation technique operates as follows. Suppose that a timing error is detected at the inputs of the combinational logic stage Sj+1, due to a delayed response of the previous stage Sj. Thus, the response of Sj+1 will be erroneous and must be corrected. Then, the evaluation time of the circuit is extended by one clock cycle and Sj+1 is fed with the delayed, but valid, response of Sj that has been captured in the MUX-latch, for error correction.

The MUX-latch is clocked by the *Memory* signal. In the error free case the *Memory* signal is exclusively controlled by the *Mem_CLK* signal, a delayed version of the clock signal *CLK* with a proper duty cycle. When the *Mem_CLK* signal is “high” the *Memory* signal is activated (turns also to “high”) and the MUX-latch enters the memory state; else the MUX-latch is transparent. The time interval hat the *Memory* signal is active must coincide with the time interval where new values arrive at the *D* inputs of the TIMED Flip-Flops, in all stage registers, due to an earlier evaluation of the pertinent logic stages according to the circuit specifications. Any signal transition at the *D* inputs of the TIMED Flip-Flops, earlier than the activation time of the *Memory* signal, is considered as violation of the timing specifications and must be detected. Obviously, the deactivation of the *Memory* signal (falling edge), and accordingly of the *Mem_CLK* signal, must occur before the triggering edge of the *CLK* signal and at a time distance at least equal to the delay time of the MUX-A plus the setup time of the Main Flip-Flop.

The XOR gate in the TIMED Flip-Flop detects timing errors and indicates them by setting signal *Error_L* to “high”. An OR gate is used to collect the *Error_L* signals and to generate the register error indication signal *Error_Rj*. Any register error indication signal is captured by a single Flip-Flop (Error Flip-Flop) triggered by the *Mem_CLK* signal which has been properly delayed. The final error indication signal, *Error*, is used to activate the error correction mechanism.

A. RANDOM TEST PATTERN GENERATION

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In this project, we also proposes the random test sequences in our experiments. These random test sequences are used to demonstrate that auto scan does not require sequential test generation in order to be effective. The random test sequences are independent of the particular auto scan configuration. They are meant to be applied to the circuit from an external source. LFSR are widely used for generating the random test sequences.

B. LINEAR FEEDBACK SHIFT REGISTER

One of the two main parts of an LFSR is the shift register (the other being the feedback function). A shift register is a device whose identifying function is to shift its contents into adjacent positions within the register or, in the case of the position on the end, out of the register. The position on the other end is left empty unless some new content is shifted into the register. The contents of a shift register are usually thought of as being binary, tat is, ones and zeroes. If a shift register contains the bit pattern 1101, a shift (to the right in this case) would result in the contents being 0110; another shift yields 0011. After two more shifts, things tend to get boring since the shift register will never contain anything other than zeroes figure 4.1 4-Bit LFSR, Tap Sequence;

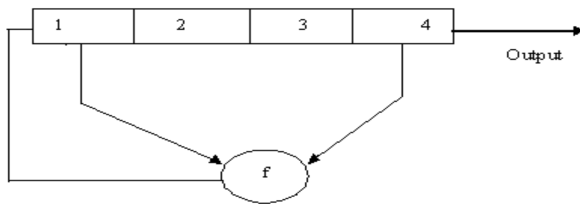

Fig.2. 4-Bit LFSR, Tap Sequence;

Two uses for a shift register are
1) Convert between parallel and serial data.
2) Delay a serial bit stream.
The conversion function can go either way fill the shift register positions all at once (parallel) and then shift them out (serial) or shift the contents into the register bit by bit (serial) and then read the contents after the register is full (parallel).

III. RESULTS

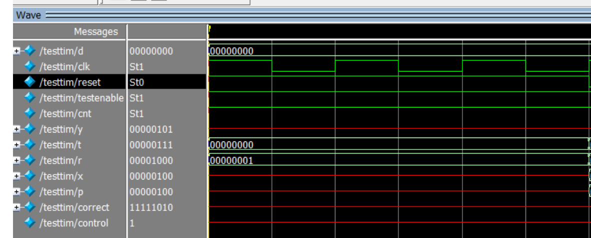

Fig.3. Simulation Result

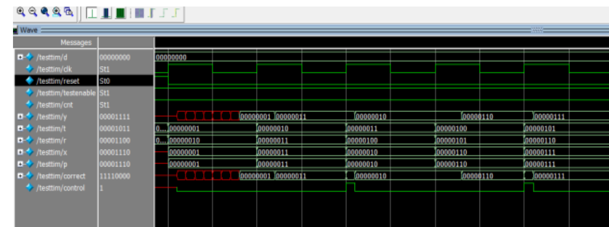

Fig.4. Pattern Generation Result

IV. XILINX SYNTHESIS REPORT

The proposed has been simulated and the synthesis report can be obtained by using Xilinx ISE 12.1i. The various parameters used for computing the proposed systems with Spartan-3 processor are given.

A. SYNTHESIS REPORT

Product Version:	ISE 12.1	• Warnings:	8 W
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	7	960	
Number of Slice Flip Flops	8	1920	
Number of 4 input LUTs	13	1920	
Number of bonded IOBs	27	66	
Number of GCLKs	1	24	

Detailed Reports

Fig .5. Existing Report

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Target Device:	xc3s100e-5vq100	• Errors:
Product Version:	ISE 12.1	• Warnings:
Design Goal:	Balanced	• Routing Results:
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:
Environment:	System Settings	• Final Timing Score:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utili
Number of Slices	2	960	
Number of Slice Flip Flops	3	1920	
Number of 4 input LUTs	4	1920	
Number of bonded IOBs	18	66	
Number of GCLKs	1	24	

Detailed Reports				
Report Name	Status	Generated	Errors	Warnings
Synthesis Report	Current	Tue Oct 10 13:50:11 2017	0	43 Warnings (40 new
Translation Report				
Map Report				

Fig .6. Proposed Report

Table.1. Comparision Table

s.no	Parameter	Existing	Proposed
1	Slice	7	2
2	Lut	13	4

V. PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction in time and area based on the implementation results which have been done by using Spartan-3 processor. The proposed algorithm significantly reduces area consumption when compared to the existing system.

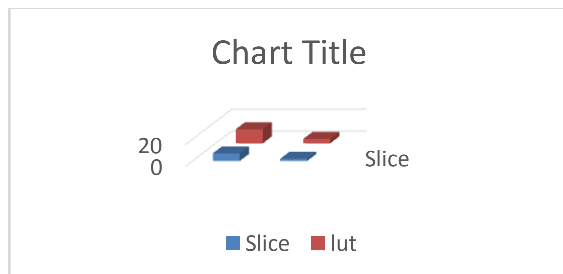

Fig.7. Performance analysis

VI. CONCLUSION

Autoscan, a design for testability (DFT) technique for synchronous sequential circuits is implemented. Autoscan gives up the external scan inputs and outputs of conventional scan in order to eliminate the test data volume associated with these lines scan operation under autoscan improve the circuit testability by allowing the circuit state to be modified through shift operation. In this existing method, due to the removal of the scan inputs and outputs, synthesis of scan chains under autoscan does not have to maintain a single direction for every scan chain. Instead, it is possible to define any number of scan chains with different directions and different sources. Autoscan is to detect almost all the faults that are detectable using conventional scans in all circuits considered. Here we can use random test sequences, because random test patterns covers more fault coverage's than sequential test patterns. In the proposed method, we have to find the delay fault by using the test pattern generation. In future using weighted test pattern generator we have to find the delay fault occur in the standard circuits.

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