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Design of 16:1 Multiplexer in Adiabatic Logic Techniques

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Abstract— In this paper, the efficiency of a fully adiabatic logic circuit is compared with its combinational and pipelined static CMOS counterparts. The performance of each circuit is studied in terms of the maximum frequency of operation, the minimum voltage of operation, the circuit energy consumption, and the switching noise generated by the circuit. Here we are designing 16:1 multiplexer using adiabatic techniques and results we got are quite effective and and helpful in low power consumption.The design simulation is done with the help of software and comparision is done with different adiabatic techniques.

I. INTRODUCTION

Highly concerned issue in the low power VLSI design is energy/power dissipation. This is due to the increasing demand of portable systems and the need to limit the power consumption in VLSI chips. In conventional CMOS circuits, the basic approaches used for reducing power consumption are by reducing the supply voltages, on decreasing node capacitances and minimize the switching activities with efficient charge recovery logic[1]. The adiabatic logic works on the principle of energy recovery logic and provides a way to reuse the energy stored in load capacitors rather than the conventional way of discharging the load capacitors to the ground and wasting this energy. The Power consumption is the major concern in low power VLSI design technology.

II. ADIABATIC LOGIC DESIGN

The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity[1]. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy [2]. It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component[3] and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems . Like many other adiabatic logic families, Reversible logic is a dual-rail logic family based upon a pair of cross-coupled inverters that are supplied using a power-clock, rather than a static DC power-supply. The configuration of the evaluation logic is what makes reversible logic an ideal family to implement fully reversible adiabatic logic [3][4]. This logic is constructed from nMOS devices attached between the power-clock and the outputs. These nMOS devices take complementary inputs and are constructed to produce a low-resistance path between the power-clock and the asserted output. The non-asserted output should be left with a high-impedance path to power-clock, and will be pulled low by the cross-coupled n-type devices. This means that the function is evaluated when there is sufficient differential between the two outputs, but far more importantly means that by using reverse-flowing data, the outputs can be more completely recovered. This should allow losses to be reduced to leakage[6].

III. NEED FOR LOW POWER

The requirement for low power design has caused a large paradigm shift where energy dissipation has become as essential consideration as area and performance. Several factors have contributed to this trend. The need for low power devices has been increasing very quickly due to the portable devices such as laptops, mobile phones and battery operated devices such as calculator, wrist watches. These products always put a large attention on minimizing power in order to maximize their battery life. Another motive for low power is associated to the high end products. This is due tothe packaging and cooling of such high performance, high density and high power chips are prohibitively expensive. Another consideration low power design is related to the environment. The Micro electronics products become tolerable usage in everyday's life, their need on energy will sharply increase. Therefore the reduction in powerconsumption reduces the heat generated and so reduces the cost required for extra cooling systems in homes and office.

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IV. OPERATION OF ADIABATIC LOGIC

The term adiabatic indicates the thermodynamics process which is used to describe a process with no transfer of heat with the environment. Hence the adiabatic logic structure effectively reduces the power dissipated in a circuit. The adiabatic switching technique can realize very low power dissipation[1]. Figure (1) shows the adiabatic switching process. Adiabatic logic offers a method to use the energy stored in load capacitors compared to the traditional method of discharging load capacitor to the ground and this energy is wasted. Thus, the term adiabatic logic implements reversible logic and used in low-power VLSI circuits.

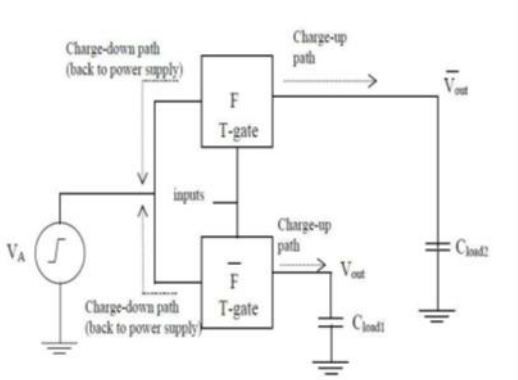

Figure 1 .Adiabatic Switching Process

V. EFFICENT CHARGE RECOVERY LOGIC

ECRL consists of two cross coupled PMOS transistors and two N-functional blocks for ECRL adiabatic logic block. Both out and out bar are generated. Energy dissipation is reduced to a large extent in ECRL logic by performing the precharge and evaluation phase simultaneously. ECRL NAND gate ECRL dissipates less energy than other adiabatic logics by eliminating the precharge diodes. It consists of only two PMOS switches[7]. It provides full swing at the output. The basic structure of ECRL logic is similar to the Differential Cascode Voltage Switch Logic (DCVSL) with differential signaling.

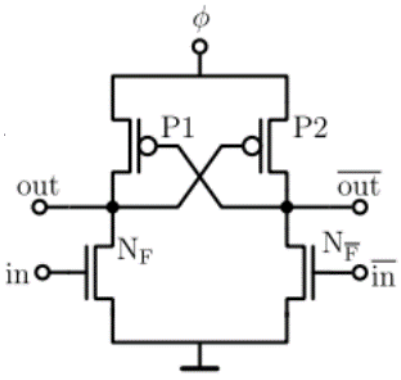

Figure 2 .ECRL NAND Logic

A major disadvantage of ECRL circuit is that the coupling effects due to the two outputs are connected by the PMOS latch and the two complementary outputs can interfere with each other.

VI. IMPROVED EFFICENT CHARGE RECOVERY LOGIC

IECRL consists of a pair of cross coupled PMOS device and two N-functional blocks. In IECRL, delay has been improved by adding a pair of cross coupled NMOS devices in the ECRL design. The basic structure of IECRL is similar to the Modified Differential Cascode Voltage Switch Logic (MDCVSL) with differential signaling.The IECRL logic is the improved ECRL logic. The performance of IECRL is better than the ECRL logic even though the number of transistors is higher than the ECRL logic[4]. The main advantage of IECRL logic is that it consists of a pair of cross coupled NMOS devices to improve the performance of ECRL logic.

VII. MULTIPLEXER DESIGN

Multiplexers are called data selectors. It has 2n inputs, n selection inputs and 1 output. Multiplexers in digital electronics are used to implement combinational functions. In communications, it is used to multiplex different signals into a single channel. In this paper we consider an 16x1 multiplexer, which has 16 inputs, 4 selection inputs and 1 output.

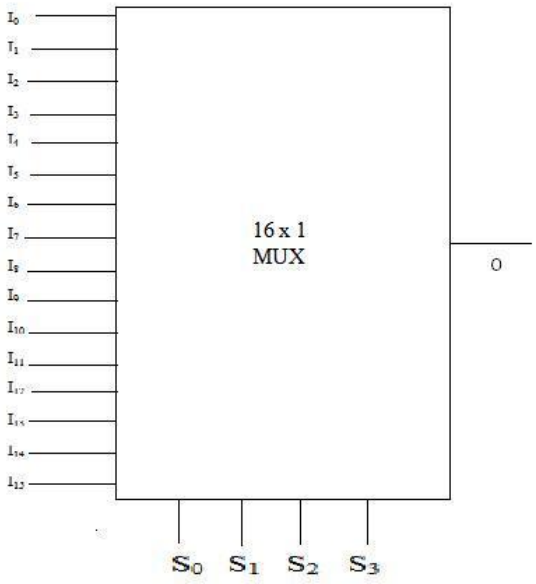

Figure 3 .Multiplexer

VIII. PROPOSED DESIGN

The proposed design of 16:1 multiplexer is designed using Adiabatic techniques namely ECRL and IECRL and their circuit and simulation is done on software namely DSCH2 of Microwind tool. Using Adibatic techniques we found less consumption in power as compared to CMOS design . These designs can be quite useful in power consumption as lot of power is wasted.Verilog file is generated and used for simulation in Microwind tool.

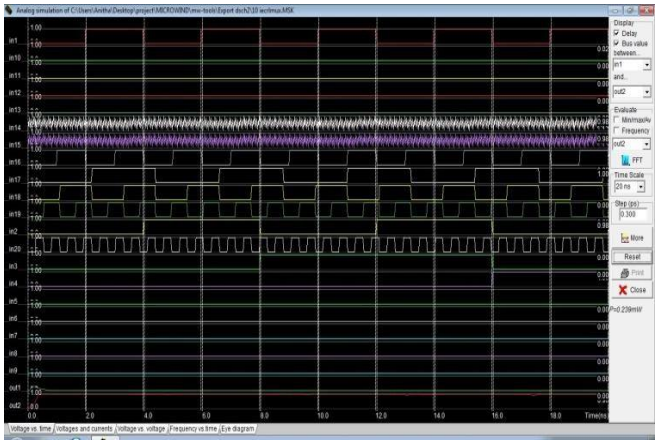

Figure 4. Schematic layout in ECRL

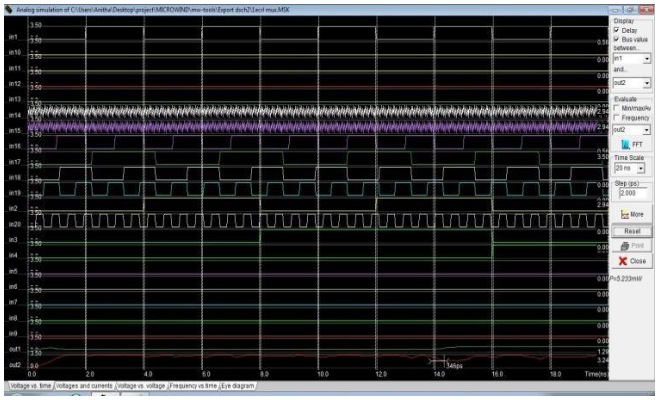

Figure 5. Schematic layout in IECRL

IX. COMPARITIVE ANALYSIS OF SIMULATION RESULTS

The simulation results are compared based on the power dissipation of the proposed circuits and their transistor count with conventional CMOS logic design. The comparison makes easier to analysis the adiabatic logic circuits based on the power dissipation. The analysis shows that the designs based on adiabatic technique offers significant power reduction which provides better power performance over conventional CMOS circuits.

Technology	Power Dissipation	Transistors
CMOS	14.23	192
ECRL	5.4	161
IECRL	0.22	164

Table 1: Comparison of 16:1 Multiplexer Using Different Logics

X CONCLUSION

Adiabatic circuits are low power solutions which will soon replace CMOS based logic circuits. From the above results, it is clearly depicted that adiabatic logic circuits reduce power dissipation with a design size penalty in terms of transistor count. Circuit simulations show that with the help of PFAL, the energy savings can be reached at a significant level. From the simulations the functionality of the implemented logic gates is found to be satisfactory.

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