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Design of Area and Power Aware Reduced Wallace Tree Multiplier

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Abstract-- Multiplier is a vital block in high speed Digital Signal Processing Applications. With the more advance techniques in wireless communication and high-speed VLSI. There are two approaches to improve the speed of multipliers namely booth algorithm and other is Wallace tree algorithm. The work has been done to reduce the area by using energy efficient Hybrid CMOS Full Adder. To implement the high-speed multiplier, Wallace tree multiplier is designed and it is a three-stage operation, which again leads to lesser number of stages and subsequently less number of transistors .Moreover the gate count is significantly reduced.

Keywords: Wallace tree multiplier, Hybrid CMOS Full adder, TANNER, 45nanometer.

I. INTRODUCTION

Fast multipliers are essential parts of digital signal processing systems. The speed of multiply operation is of great importance in digital signal processing as well as in the general purpose processors, especially since the media processing took off. In the past multiplication was generally implemented via a sequence of addition, subtraction, and shift operations. Multiplication can be considered as a series of repeated additions. The number to be added is the multiplicand, the number of times that it is added is the multiplier, and the result is the product. Each step of addition generates a partial product. In most computers, the operand usually contains the same number of bits. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content. This repeated addition method that is suggested by the arithmetic definition is slow that it is almost always replaced by an algorithm that makes use of positional representation. It is possible to decompose multipliers into two parts. The first part is dedicated to the generation of partial products, and the second one collects and adds them. The basic multiplication principle is two folds i.e., evaluation of partial products and accumulation of the shifted partial products. It is performed by the successive additions of the columns of the shifted partial product matrix. The 'multiplier' is successfully shifted and gets the appropriate bit of the 'multiplicand'. The delayed, instance of the multiplicand must all be in the same column of the shifted partial product matrix. They are then added to form the product bit for the particular form. Multiplication is therefore a multi operand operation. Power dissipation is recognized as a critical parameter in modern VLSI design field. To satisfy MOORE'S law and to produce consumer electronics goods power efficient, and reduce weight, low power VLSI design is necessary. Dynamic power dissipation which is the major part of total power dissipation is due to the charging and discharging capacitance in the circuit. The golden formula for calculation of dynamic power dissipation is $Pd = ClV2f$. Power reduction can be achieved by various manners like reduction of output capacitance Cl, reduction of power supply voltage V, reduction of switching activity based on frequency f.

II. LITERATURE REVIEW

[1]Jin-FaLin,Yin-TsungHwang,Ming-HwaShe(2012). In this paper, we propose a multiplier and compressors based on degenerate pass transistor logic (PTL). Threshold loss problem are the main drawback in most pass transistor logic family. This threshold loss problem can be minimized by using the complementary control signals. These complementary control signals are obtained by5-Transistor XOR-XNOR module. New approach of Degenerate pass transistor logic is used in the design of Compressor to reduce the Threshold loss problem, power dissipation and signal degradation at the output. The transistor level implementation of compressor and multiplier are simple, lesser power dissipation and high speed compared to other pass transistor logics .The tradeoffs ofmultipliers are in terms of power dissipation and area.

[2] Mohammad Hossein Moaiyeri and Reza Faghih Mirzaee, Keivan Navi(2009)Two new low-power, and high-performance 1-bit Full Adder cells are proposed in this paper. These cells are based on low-power XOR/XNOR circuit and Majority-not gate. Majority-not gate, which produces Cout(Output Carry), is implemented with an efficient method, using input capacitors and a static CMOS inverter. This kind of implementation benefits from low power

consumption, a high degree of regularity and simplicity. Although low power consumption has been targeted at the circuit design level for both cells, simulation results show great demonstrated improvement of proposed cells in terms of power consumption and also PDP, in comparison with the eight modern Full Adder cells.

[3] Afshin Abdollahi, Farzan Fallah, and Massoud Pedram (2004) reducing the leakage current of a CMOS circuit.In both cases, it is assumed that the system or environment produces a "sleep" signal that can be used to indicate that the circuit is in a standby mode. Dynamic power dissipation is more and negative feedback is available.

[4] Asif Jahangir Chowdhury, Shahriar Jalal Nibir and Md. Rifat Alam Siddique (2012) we propose a new method to reduce static power in the CMOS VLSI circuit using stacked sleep transistor without being penalized in power delay product requirement and circuit performance Propagation delay is more and negative feedback is available.

[5] Jonathan P. Halter and Farid N. Najm (1997) The proposed design changes consist of minimal overhead circuitry that puts the circuit into a "low leakage standby state," whenever it goes into standby, and allows it to return to its original state when it is reactivated. The area consumption is more and 180nm technology is used.

III. PROPOSED WORK

In a proposed system we design the Wallace tree multiplier with Hybrid adder technology which is used to improve the performance of the circuit and reduce the power consumption of the circuit.

A. Hybrid-CMOS design style

The designs for full adder featuring hybrid-CMOS design style. The quest to achieve a good drivability, noise-robustness and low energy operations guided our research to explore hybrid-CMOS styled sign. Hybrid-CMOS design style utilizes various CMOS logic style circuits to build new full adders with desired performance. We also classify hybrid-CMOS full adders into three broad categories based upon their structure. Using this categorization, many full adder designs can be conceived. The new full adder is based on XOR-XOR Hybrid CMOS model that gives XOR and XOR full swing output simultaneously

B . XOR-XOR based full adder

In this category, the Sum and Carry outputs are generated by the following expression, The output of the sum is generated by two consecutive two-input XOR gates and the output is the output of a 2-to-1 mux with the select lines coming from the output of Module-I. The Module-I can be either a XOR–XNOR circuit or just a XOR gate. In the first category, both Module-1and Module-II consist of XOR gates. In the first case, the output of the XOR circuit is again XORED with the carry from the previous stage in Module- II. The H and H¢ outputs are used as multiplexer select lines in Module-III.

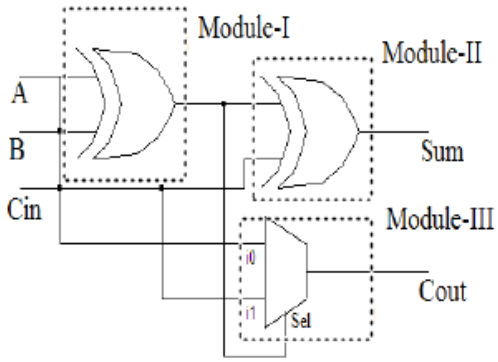

Fig.1.XOR-XOR Full adder

IV. RESULTS

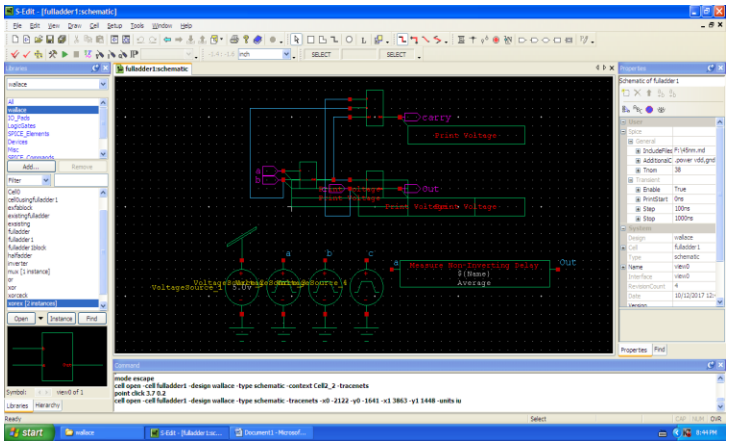

Fig.2. Proposed Full adder Circuit

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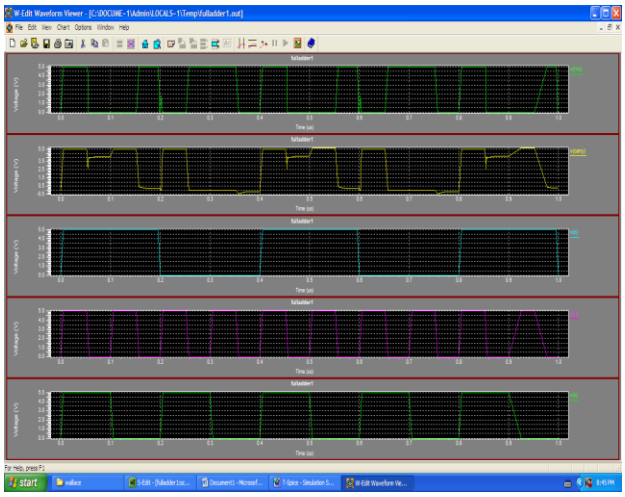

Fig.3.Proposed Full adder Output

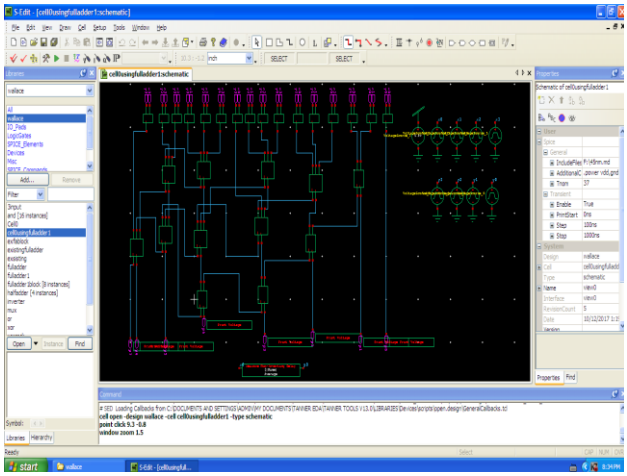

Fig.4. Proposed Wallace tree multiplier

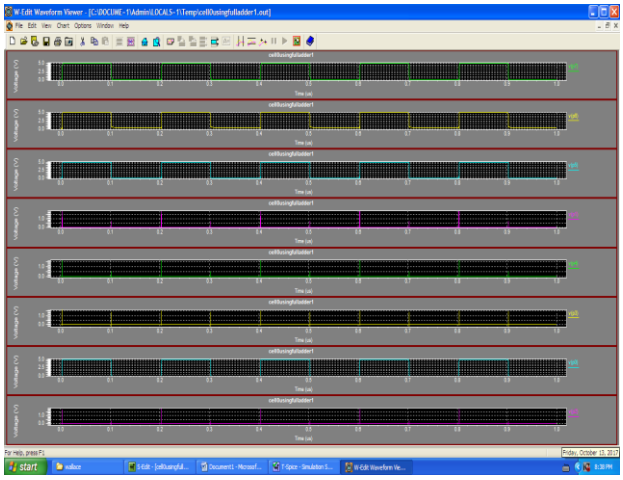

Fig.5.Output waveform

Comparison Of Existing and Proposed System

CIRCUIT	DELAY	POWER	AREA
Existing Normal Full Adder	-0.235nS	0.00572W	42T
Proposed Full Adder	-0.238nS	0.00572W	14T
Existing Normal Wallace Tree Multiplier	0.110nS	0.0704W	480T
Proposed Wallace Tree Multiplier	0.193nS	0.00276W	256T

V. CONCLUSION

In this work, Full adder and Wallace tree multiplier's transistor count is reduced from 42T to 14T and 480T to 256T which results in reduction of power consumed by these circuits. Further, by reducing the delay occurring in a circuit the speed of operation is improved

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