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Low power high efficiency SRAM using 6T

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Abstract-- SRAM Plays a major role for memory based applications in the range of large static noise margin. The noise present at the SRAM causes read and write operation delays. The level for this noise margin reaches the ability of the read and write data stability. In this paper it is needed to estimate the noise margin level and the stability of the 6T SRAM while on the read and write mode of operation. The 6T-SRAM with virtual ground is used to reduce the dynamic power dissipation from the transistor at the read and write operation. The data given to the circuit causes more stability and reliability for the high Static noise margin. The circuit is to designed at 45 nm CMOS process and analyzed in TANNER.

Keywords:6T SRAM,45 nm process, Tanner, CMOS inverter

I. INTRODUCTION

Digital systems are highly complex at their most detailed level. They may consist of millions of elements i.e., transistors or logic gates. For many decades, logic schematics served as thengua franca of logic design, but not anymore. Today, hardware complexity has grown to such a degree that a schematic with logic gates is almost useless as it shows only a web of connectivity and not functionality of design. Since the 1970s, computer engineers, electrical engineers and electronics engineers have moved toward Hardware description language (HDLs). Digital circuit has rapidly evolved over the last twenty five years .The earliest digital circuits were designed with vacuum tubes and transistors. Integrated circuits were then invented where logic gates were placed on a single chip. The first IC chip was small scale integration (SSI) chips where the gate count is small. When technology became sophisticated, designers were able to place circuits with hundreds of gates on a chip. These chips were called MSI chips with advent of LSI; designers could put thousands of gates on a single chip. At this point, design process is getting complicated and designers felt the need to automate these processes. With the advent of VLSI technology, designers could design single chip with more than hundred thousand gates. Because of the complexity of these circuits computer aided techniques became critical for verification and for designing these digital circuits. One way to lead with increasing complexity of electronic systems and the increasing time to market is to design at high levels of abstraction. Traditional paper and pencil and capture and simulate methods have largely given way to the described UN synthesized approach.

II. LITERATURE REVIEW

[1] Kasim. R, Connor. C,Hicks. J ,Jopling. J,Litteken.C This paper addresses several key aspects of integrated reliability for the Intel 45 nm logic technology with high-K metal gate (HK + MG) transistors and Pb-free packaging TDDB and (BTI) tests were implemented to enable very high sampling rates. Careful integration and manufacturing innovations were needed to meet historical expectations for transistor, defect, and package reliability and the stability of intrinsic and defect reliability performance needed to be demonstrated.

[2] Khalil, D.E; Dept. of Electr. Eng. & Comput. Sci., Northwestern Univ., Evanston, IL ; Khellah, M,Nam-Sung Kim,Ismail.Y. In this paper, an accurate approach for estimating SRAM dynamic stability is proposed. Using SNM and quasi-Monte Carlo simulation drawbacks are eliminated by employing a new distribution-independent, most-probable-failure-point search technique for accurate probability calculation along with accurate simulation-based dynamic failure criteria For different dynamic circuit techniques, such as dynamic write-back the conventional methods are not applicable.

[3] Kasim. R, Connor. C,Hicks. J ,Jopling. J,Litteken.C This paper addresses several key aspects of integrated reliability for the Intel 45 nm logic technology with high-K metal gate (HK + MG) transistors and Pb-free packaging TDDB and (BTI) tests were implemented to enable very high sampling rates. Careful integration and manufacturing innovations were needed to meet historical expectations for transistor, defect, and package reliability and the stability of intrinsic and defect reliability performance needed to be demonstrated.

[4] Zheng_Guo,Dept. of Electr. Eng. & Comput. Sci., Univ. of California,Berkeley, CA, USA ; Carlson. A.,Liang-Teck_Pang,Duong,.K.T. This paper work presents a method for large-scale characterization of read stability and writeability in functional SRAM arrays using direct bit-line measurements.A test chip is implemented in a 45 nm CMOS process. Correlation to conventional SRAM read/write metrics as well as V_{MIN} measurements near failure.

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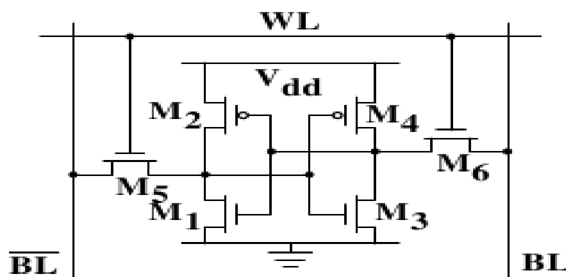
[5] Jian Wang,Yaldiz.S,Xin Li,Pileggi.L.T. SRAM parametric failure analysis . This aims at extraction for SRAM parametric failures using a controlled sampling scheme and a nested Monte Carlo analysis method. The failure probability extraction at cell-level and array-level. The SRAM failure analysis are accelerated significantly.

III. PROPOSED WORK

6T SRAM deign based on idle mode operation Data is read and written from BL (Bit line) through transmission gate whose controlling signals are WL and WLB (Word lines). During idle mode of cell transmission gate is OFF. When ‘1’ is stored in cell, Transistor NM1 is ON and STB node pulled down to GND. Bit ‘1’ is stored at ST node uses leakage current from BL through transmission gate and storage of charge at the node due to various capacitances of MOS transistor and wires.



Fig,1. 6T SRAM

IV. RESULTS

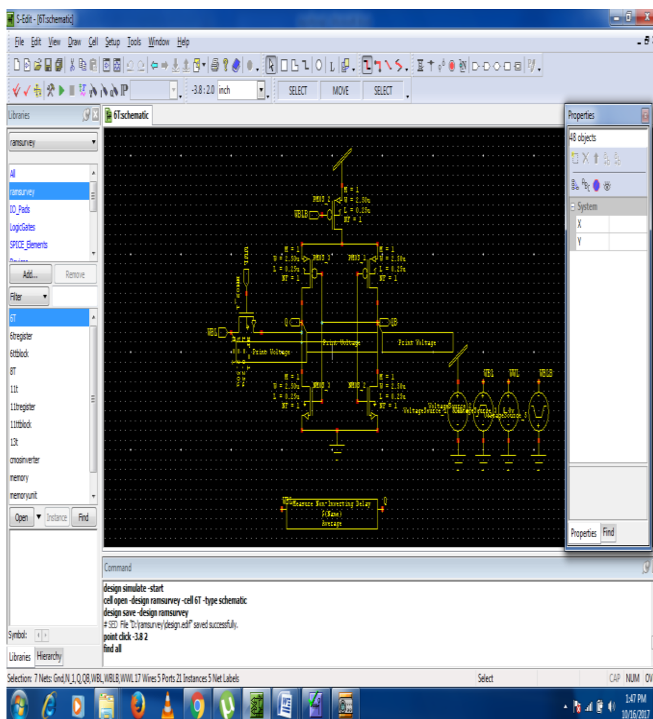


Fig.1. 6T SRAM CIRCUIT

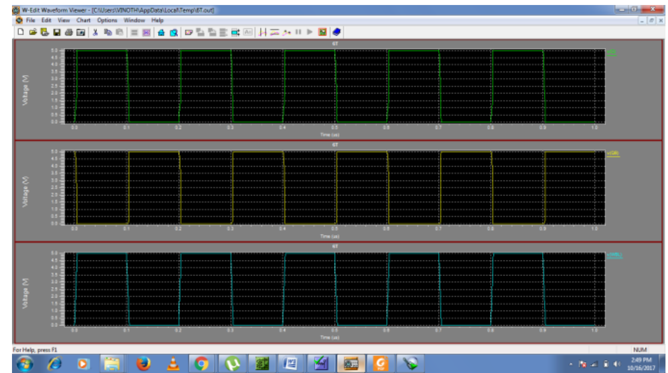


Fig.3.Output Waveform

Comparision Table

	AREA	POWER	DELAY
13T SRAM	13T	0.00281w	0.597ns
11T SRAM	11T	0.01081w	0.0106ns
8T SRAM	8T	0.00665w	0.381ns
6T SRAM	6T	0.000115w	0.95ns

V. CONCLUSION

We design and study the multiple SRAM circuit using the 13transistor,11transistor,8transitor and 6 Transistor and measure the power and delay of those circuit from our survey we detect the 6T one is best one so we implement the 6T SRAM register by using the 6T SRAM register we implement the memory element.

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