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ECG Acquisition System with 0.3V Supply Using Digital Front-End Architecture

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***Abstract*— This intended work presents an electrocardiogram acquisition system with power efficiency that makes use of a fully digital architecture inorder to reduce the consumption of power and area of the chip. The proposed digital architecture is compatible with CMOS technology and it can operate with a low supply voltage of 0.3 V. In this architecture, analog block, e.g.,low-noise amplifier (LNA), and filters, and passive elements, such as ac coupling capacitors, are not used. Instead of the LNA and antialiasing filter, a moving average voltage-to-time converter is used. Inorder to cancel the impact of the dc offset on the circuit, a digital feedback loop is employed which also eliminates the need for coupling capacitors.**

***Index Terms*— Anti-aliasing, Area efficient, Digitization, Electrocardiogram (ECG), Grey wolf optimization, Moving average filtering, Offset cancellation.**

I. INTRODUCTION

Electrocardiogram (ECG) is a diagrammatic recording of electrical current through the heart for a period of time. This biological signal, is generally used for diagnosis of some diseases by analyzing the signal. Each portion of the ECG waveform usually carries information that is appropriate for a clinician in order to arrive for a proper diagnosis. Due to external noises, there are chances of ECG signal that is taken from a patient getting corrupted hence it is necessary to obtain a proper noise free ECG signal. In all applications, firstly preconditioning and conversion of biosignal to digital is done. Processing of the digital data for monitoring or diagnosis applications is performed by a digital signal processor. Biomedical signal acquisition systems generally consist of a low-noise amplifier (LNA), a band pass filter, an analog sample-and-hold, and an analog-to-digital converter (ADC). Normally the analog devices consume more amounts of power and area. Digitization is a process of converting information into a digital format, usually in terms of bits and plays a crucial role in today's life. They have important applications in virtually all fields of human activity and have a global influence on the performance of society. Digitization also finds importance in data processing, storage and transmission i.e., it allows information of all kinds in all formats to be carried with the same efficiency, unlike analog data, which typically suffers some loss of quality each time, it is copied and transmitted. Another advantage is the speed in which information can be transmitted without degradation. Automated ECG interpretation uses artificial intelligence and pattern recognition software used for interpretation, test reporting and diagnosis of ECG tracings usually from a patient. Each of these recordings is then digitized by means of ADC and special data acquisition software or DSP chip. Resulting digital signal is processed by a series of specialized algorithms to remove noise, etc. Mathematical analysis is now performed on the clean signal of all channels, to identify and measure a number of features which are important for interpretation of PQRST wave usually called feature extraction. Pattern recognition makes use of rule based systems, cluster analysis are used to derive conclusions, interpretation and diagnosis. Later a reporting program is activated and produces a proper display of original and calculated data as well as results of automated interpretation Although there is an advancement of CMOS technology, that enables scaling to the lower power consumption and higher performance in digital circuits many parameters like Signal-to-Noise Ratio (SNR), dynamic range and gain of the analog parts of an IC are negatively impacted. Therefore, it is desirable to find a new architecture in which more digital blocks are used. One such is used in the proposed system functions implemented by analog blocks are performed by digital circuits. By using this approach, flexibility of the system can be increased by removing unwanted interferences and moreover, digital calibration techniques can be used more easily.

As seen in the biomedical signal acquisition systems, the amplifier consumes most of the power and is the only analog block that is used. Hence, it can be replaced with an appropriate digital block, thus the circuit will be more competent in terms of power. However, there are other issues that have to be addressed before moving towards the fully digital implementation. Two of the issues are as follows:

1) Removing the DC Offset Voltage of Electrodes without using Passive Elements.
2) Providing a Solution for Anti-aliasing Filter.

Motivated by the above-mentioned issues, we have designed a new fully digital electrocardiogram (ECG) signal acquisition system that operates by a supply voltage of 0.3 V. Using the proposed architecture, the area and power consumption is reduced. In Section II, the architecture of the proposed fully digital front end is introduced. In Section III,

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flow chart of the proposed system is discussed, and the MATLAB simulation results and observation are presented in Section IV. Finally, the conclusion is drawn in Section V.

II. PROPOSED FULLY DIGITAL FRONT-END ARCHITECTURE

The overall block diagram of the proposed fully digital architecture is as shown in Fig 1(a).The advantages of digital CMOS technology are utilized hence in this structure, the processing of the biosignal is performed in the time and digital domain. Using voltage-to-time converter (VTC) the analog biosignal which is coming from the electrode is converted to time and is directly connected to the front-end circuit. From this point on in the circuit, the signal information and VTC output signal are in the phase. The output of the VTC is applied to the time-mode processing block, in which antialiasing and offset cancellation are done in time domain. Then, a time-to-digital converter (TDC) transfers the time-mode signal into digital domain where other processes (digital filtering, data compression/reduction, and so on) are performed.

In Fig 1(b) shows the proposed digital architecture. It consists of an active electrode, two digital-to-current converters (DCCs), a moving average VTC (MA-VTC), a control logic block, a counter, and a demultiplexer. In this architecture, the impact of the electrode offset on the circuit is cancelled via a feedback loop and ac coupling capacitors are removed.

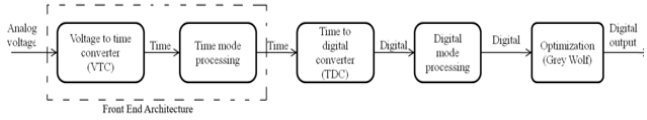

Fig 1(a): Overall block diagram of the proposed system.

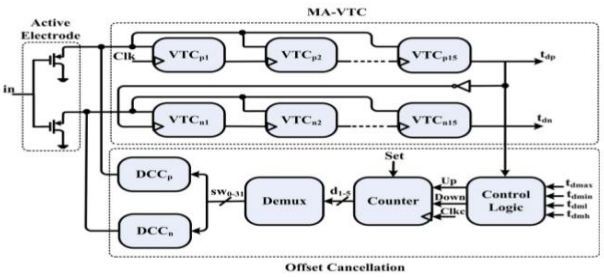

Fig 1(b): Proposed digital front-end architecture.

A. Active Electrode: An active electrode is an electrode, in which some active elements are used to reduce the power line interference. Fig. 2 shows two different two-wired active electrodes for comparison. The circuit in first figure uses an op-amp, while the second one is implemented using a single transistor. Important parameters of such electrodes, such as offset, noise, gain, and output resistance, are compared. It is shown in that the transistor circuit has a superior performance in terms of noise, common mode rejection ratio (CMRR), and power consumption. However, the offset and the output resistance are worse. The most important limiting factor in ECG application is the input noise of the system, hence active electrode with a single MOS transistor is used.

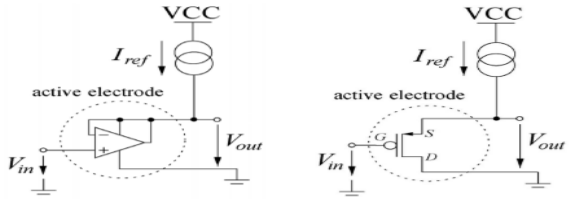

Fig 2: Active electrode with either an op-amp or a MOS transistor, both operating as a voltage follower.

B. Voltage to Time Converter (VTC): The analog input voltage is converted to a measurable time via a VTC at the first stage in the proposed digital implementation. The signal information is now in the delay of the clock signal (CLK). The VTC should be designed in such a way that the small amplitude of the input voltage generates a large enough delay, linearly. We have used both the positive and the negative VTCs in our design to implement a moving average filter (as will be explained later). The cascaded stages of VTCs form delay-line structures. In addition, the delay line structure introduces time-domain amplification into the design. In particular, the input signal can be amplified in the time domain by simply extending the time window (using more VTC stages). This is in contrast to voltage amplification involving complicated analog amplifiers in the conventional systems. The sampled input voltage Vin is first converted to a time window T (Vin), which is then quantized by TDCs. This design is suitable for high-resolution applications.

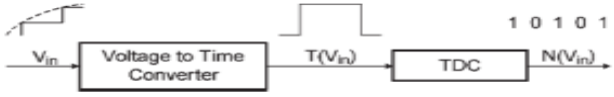

Fig 3: Voltage- to-time-to-digital conversion.

C. Moving Average Filtering**:** Because VTCs work with a clock and are broadband compared with the signal bandwidth, out-of-band noise aliasing would be caused if an antialiasing filter is not used before VTCs. In order to prevent aliasing and to avoid having an analog filter in the design, we have developed the structure shown in Fig. 4 for converting the voltage-to-time as well as acts as antialiasing filtering. In this structure, a series of 15 positive VTCs are followed by another series of 15 negative VCTs. A sinc function is generated in this configuration and it behaves similar to an antialiasing filter.

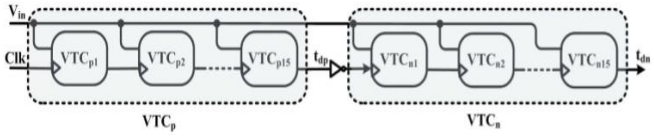

Fig 4: Schematic of the MA-VTC circuit

Each VTC in the chain integrates the signal over a limited period of time which usually depends on the delay of that VTC. For example, the first VTC integrates the signal from the rising edge of the clock to the time equal to the delay of this VTC. The second VTC integrates the signal from the rising edge of the output of the first VTC over a time period determined by its delay.This occurs for all the VTCs in the chain. The sum of these integration periods and the clock

period are equal. Hence, the representation of the integration over this time window can be,

$$Y(Ts,t) = \frac{1}{Ts}\int_{t-Ts}^{t} \mathrm{Vin}(\tau)\mathrm{d}\tau. \quad (1)$$

Therefore, a rectangular pulse in the range of [0,Ts] is its impulse response,

$$h(t) = \frac{1}{Ts}\int_{t-Ts}^{t} \delta(\tau)\mathrm{d}\tau = \mathrm{u(t)} - \mathrm{u(t-Ts)} \quad (2)$$

Hence, sinc function becomes its frequency response,

$$H(j\omega) = \frac{2\sin\left(\left(\frac{\mathrm{Ts}}{2}\right)\omega\right)}{\omega \mathrm{Ts}} \quad (3)$$

In this way, the moving average filtering is embedded in the MA-VTC thereby preventing aliasing of the wideband noise.

D. Clock Frequency and Signal Recovery: Designing of VTCp and VTCn blocks are done in such a way that the absolute slopes of their characteristic curves are equal. Hence, for any input voltage, we can write

$$\mathrm{tdp} + \mathrm{tdn} = \mathrm{ttot} = \mathrm{Constant} \quad (4)$$

The delay time tdp (or tdn) of a VTC gate is supposed to be a linear function of its input voltage and is given by

$$\mathrm{tdp} = \alpha\mathrm{Vinp} + \beta 1 \quad (5)$$

$$\mathrm{tdn} = -\alpha\mathrm{Vinn} + \beta 2 \quad (6)$$

where Vinp and Vinn are the input voltage during the time interval that the clock pulse passes through VTCp and VTCn, respectively. In addition, α, β1and β2 are constants. Tclk, the clock period, should be chosen such that for the maximum variation of the input tdn is always measurable and is not zero. This indicates that the clock period should be slightly more than ttot. Hence,

$$\mathrm{TCLCK} \geq \mathrm{tdp} + \mathrm{tdn} = \alpha(\mathrm{VinpVinn}) + \beta 1 + \beta 2 \quad (7)$$

The digital front end outputs are tdp and tdn. These delays are converted by two TDCs to two digital numbers (DP and DN). The digital number corresponding to the input voltage, Din, can be obtained from

$$\mathrm{Din} = \frac{\mathrm{Dp} - \mathrm{Dn}}{2\mathrm{D}\alpha} + \frac{(\mathrm{D}\beta 2 - \mathrm{D}\beta 1)}{2\mathrm{D}\alpha} \quad (8)$$

where Dα, Dβ1, and Dβ2 are digital numbers of α, β1, and β2, respectively.

E. DCCs Circuit : Depending on the 32-bit digital number (SW0 to SW31) at the output of the Demux, a current is generated by these blocks. Fig.5 shows the DCC circuit, in which gate voltages that are generated by the lower circuit is required for the reference current generator in the upper circuit. The transistors of the DCC are sized so that Vinp and Vinn are changed in such a way that the impact of the offset at the input of the active electrode as well as that of the VTC and DCC blocks are cancelled. For better understanding the behavior of the DCC assume that the offset at the input increases (decreases) leading to a rise (fall) in Vinp andVinn. As a result, the delay of the VTCp block increases (decreases) and that the VTCn decreases (increases). Delay variations are sensed by the TCs in the control block and a new control bit is generated by the counter and Demux. Consequently, Vinp and Vinn are reduced by 3.125 mV and one of the current controlling transistors (M1p to M32p for the DCCp and M1n to M32n for the DCCn) are turned ON.

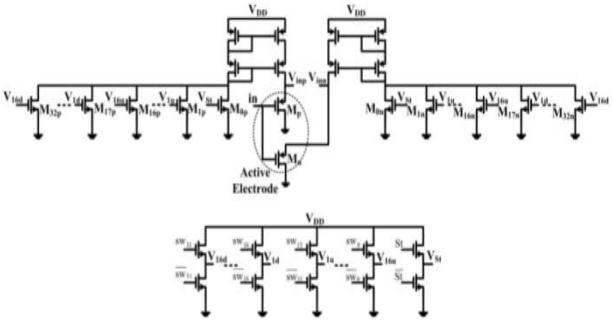

Fig 5: Structure of the current DCCs.

F. Control Logic : The control logic diagram is shown in Fig 5. It consists of TCs, AND and OR gates, and set-reset (SR) latches. For detecting the offset, the control logic should compare tdp with four predefined delays (tdmax, tdmin, tdml, andtdmh). Note that in an analog front end, for detecting the offset voltage, an analog voltage comparator should be used. In our design,the offset is detected by TCs, which are implemented by D flip-flops and are more power and area efficient compared with the analog voltage comparators. The outputs of the control logic circuit are the UP and DOWN signals, which control the up/down counter in the offset cancellation block. The counter in our design is implemented by NAND gates and jk flip-flops.

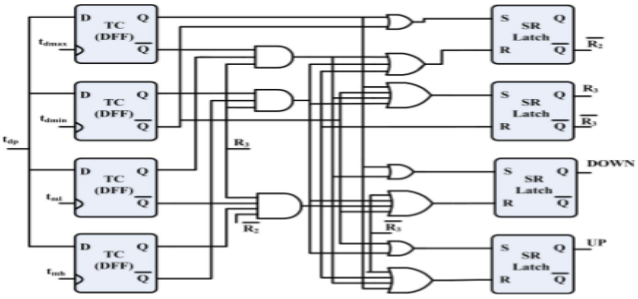

Fig 6: Schematic of the control logic

G. Offset Cancellation: Offset cancellation block is composed of two 5-bit DCCs, control logic, 5-bit counter, 5-32 bit demultiplexer. Output delay of VTCp block tdp is compared with tdmax and tdmin(predefined delays) in the control logic block by a TC to determine the operation region of VTCp. If delay is more(less) than tdmax(tdmin) the DOWN(UP) signals will be set by the control logic block. Output of Counter changes accordingly and is applied to the Demux, which controls the DCC. DCC are in charge of generating a current that depends on 32-bit digital number at the output of the demux.

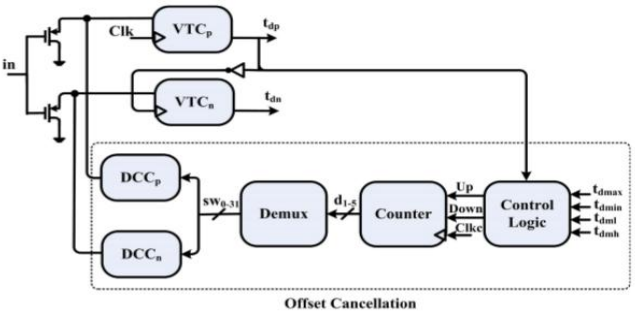

Fig 7: Offset cancellation

F. Grey Wolf Optimizer: It is a population based on meta heuristics algorithm that simulates the leadership hierarchy and hunting mechanisms. Grey wolves are considered as apex predators, which are at top of the food chain. Usually live in groups called packs. First level in hierarchy are the alpha wolves and are the leaders of the pack, responsible for making decisions about hunting, time to walk, sleeping place ,so on. Second level are the beta wolves, these are subordinate wolves which help the alpha in decision making. They reinforce the alpha's commands throughout the pack and give the feedback to alpha. Third level is the delta wolves, they have to submit to alpha and beta but dominate the omega. They are responsible for watching the boundaries of the territory and warming the pack in case of any danger, so on. Fourth level is omega wolves, they are considered the scapegoat in the pack, and they have to submit to other dominating wolves. Fittest solution is alpha, second and third fittest is beta and delta.

GWO Algorithm

Initialize the grey wolf population Xi (i = 1, 2,……..n)
Initialize a, A, and C.
Calculate the fitness of each search agent
Xα=the best search agent
Xβ =the second best search agent
Xδ =the third best search agent
while (t < Max number of iterations)
for each search agent
Update the position of the current search agent by above equations
end for
Update a, A, and C
Calculate the fitness of all search agents
Update Xα, Xβ , and Xδ
t=t+1
end while
return

III. Flow Chart

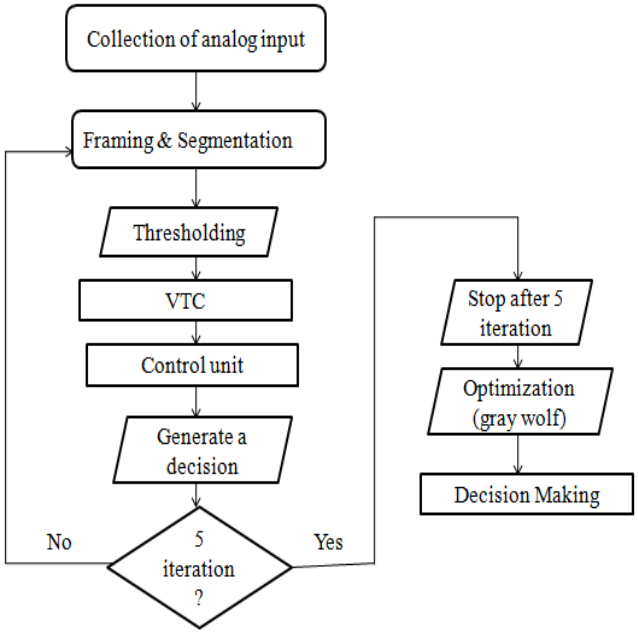

Fig 8: Flow chart

The analog input is collected from the active electrode and is then framed and segmented in the next block. These frame and their corresponding segments are fed to a threshold block, this block checks on whether equal amount of signal is divided or not. In the VTC block, the analog input voltage is converted to a measurable time, along with this block when a control unit is added it becomes a decision making block. But the decision generated is not considered to be the final decision. These above steps are redone for several fragments and their segments. On stop or on manual intervention, segments are passed through optimization block where the packs communicate with each other and arrive at a point on the exact ECG signal. For signal demonstration and output analysis software tool TANNER is used with digitized file generator (*.txt).

IV. Results and Observation

The schematic representation of the test bench is as shown in the Fig 9, consisting of complete clock circuitry, modulated circuits and a constancy circuit. Fig 10 shows the final stage of simulation output with analog, threshold, VTC and digital signals merged. Fig 11 shows the output of the test bench separately.

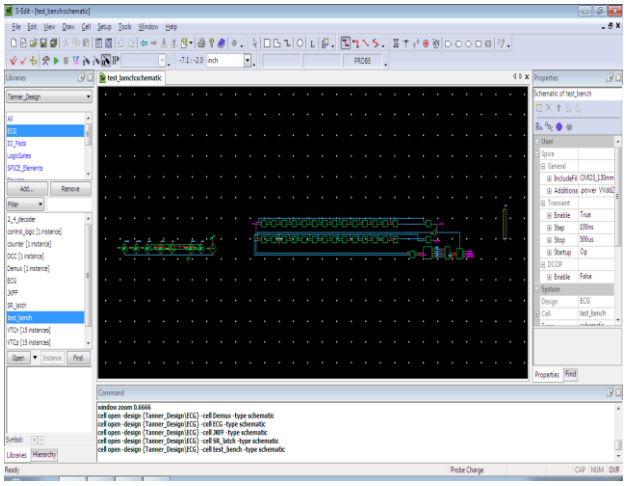

Fig 9: Schematic representation of Test bench

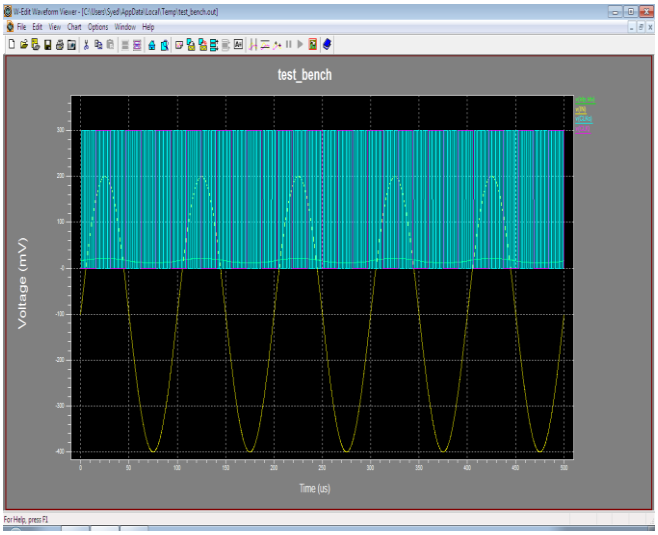

Fig 10: Simulation output

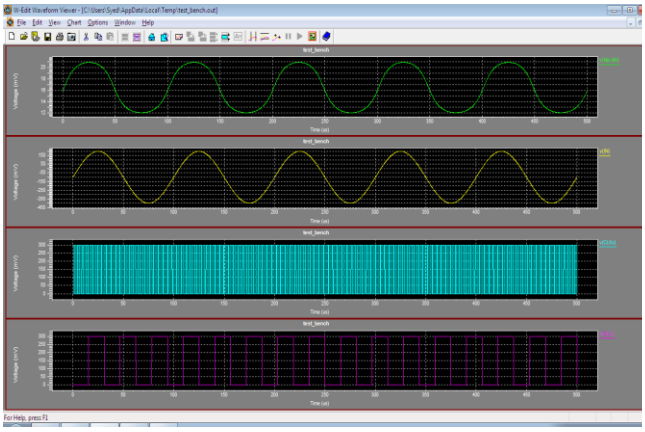

Fig 11: Test bench output

V. CONCLUSION

In the current era of rapid digitization, a fully digital front-end architecture for an ECG acquisition system was designed. Conversion of ECG signals from their analog morphological structures to a digitalized file is considered a major challenge. Typically a proportion of 0.5V is required to convert an ECG signal to its digitized form hence, creating a major setback in power consumption. A Proposal of power optimization from 0.5V to 0.3V is worked under this segment. This research includes recalibration, optimization and reclustering of previously designed system with respect to power optimization.

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